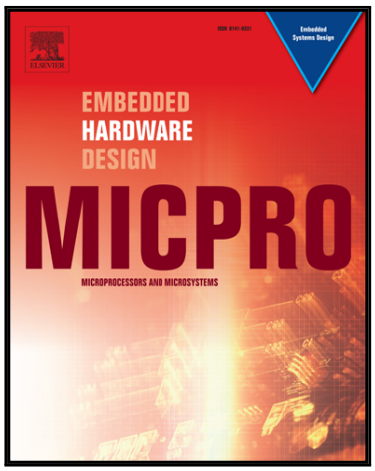

A low-power wireless-assisted multiple Network-on-Chip

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A low-power wireless-assisted multiple Network-on-Chip

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Abstract

Multiple network-on-chip (Multi-NoC) architectures are supposed to distribute the network traffic categorically among disjoint sub-networks. The main objective is significant energy reduction through power-gating of unused sub-networks. However, the packets are delayed due to sleep/wake cycles, which directly influences the overall performance of the system. In addition, the communication infrastructure of the Multi-NoC should be selected carefully to avoid performance degradation. Our solution to address these issues is using wireless links, which is used to relax the timing restrictions on sleep/wake cycles to save more power without losing performance. To realize wireless communications, we adopt two types of on-chip wireless technology that operate at different frequency bands, namely terahertz (THz) and millimeter-wave (mmW). To evaluate the merits of the proposed architecture that employs these wireless technologies, we used both real application benchmarks (PARSEC and SPLASH-2) and synthetic traffics on a many-core processor. For THz technology, the proposed architecture results in nearly 51% and 10% power reduction compared to traditional single network-on-chip (Single-NoC) and a power-gated 4-subnets Multi-NoC respectively. The corresponding results for mmW technology show 46% and 6% power reduction. Also, the proposed architecture for THz and mmW technologies results in 10% and 7% latency reduction compared to Multi-NoC

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