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Constructing in-chip micro-supercapacitors of 3D graphene nanowall/ruthenium oxides electrode through silicon-based microfabrication technique

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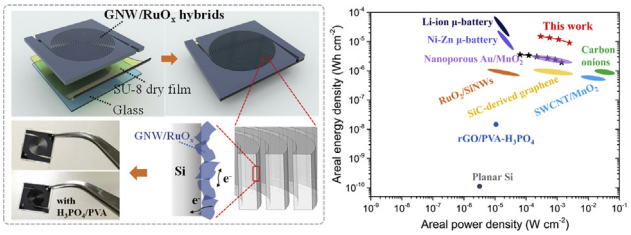
HIGHLIGHTS

- Microsupercapacitor made using 3D graphene/RuO_x coated silicon micro-electrode.
- Device production is compatible with silicon-based microfabrication process.
- Design Strategy to embed nanomaterial inside chip to favor device encapsulation.
- High areal capacitance and cyclability without sacrificing power performance.

GRAPHICAL ABSTRACT



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ABSTRACT

The rapid development of sensor networks for smart industry requires comparable tiny power sources that can deliver high energetic performance and be mass-produced via the existed semi-conductor process. In this paper, novel 3D in-chip micro-supercapacitors (MSCs) based on hierarchical electrodes were developed through silicon-based microfabrication techniques by depositing graphene nanowall (GNW)/ruthenium oxides (RuO_x) core-shell hybrids on the silicon scaffolds that are generated from deep reactive ion etching (DRIE). Conformal coating of RuO_x on individual graphene nanoflakes was realized via reactive sputtering technique to benefit capacitance enhancement, while the orderly aligned GNW facilitated fast ions and electrons transfer. By harnessing both the merits of huge active surface area of the 3D hierarchical electrode architectures and the excellent electrochemical behaviors of the GNW/RuO_x hybrids, the assembled MSCs exhibited areal energy, power densities of 15.1 μWh cm^{-2} and 2.49 mW cm^{-2}, respectively. In parallel with our novel in-chip strategy by leveraging the bulk volume of Si substrate to create sidewall for effective area enhancement at footprint, the embedment of electrode nanostructures inside the substrate may also give a new concept of MSCs design towards protecting the fragile electrode materials and making the subsequent device encapsulation with ease.

1. Introduction

The booming trends toward real-time and sustainable operation of sensor networks for the Internet of Things (IoT) have sparked dramatic increasing demands on energy autonomy [1,2]. Albeit the advent of energy harvesters presents an ideal solution by capturing the power

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from renewable ambient sources, their weak and intermittent output feature require a complementary energy storage unit that can deliver peak power and sustain repeated charge-discharge [3]. Micro-supercapacitors (MSCs) have been identified as a promising candidate for this purpose due to their superior power densities and cycling lifetime than that of battery counterparts [4]. Practical application scenarios of high-density integration and system-in-package (SiP) require the MSCs not only to be fabricated by leveraging the silicon-based semiconductor or micro-electro-mechanical system (MEMS) fabrication techniques, but also to be operated with high energetic performance at the footprint area [5].

Study to date have shown amount of reports on MSCs with diverse nanostructured electrode materials. Among them, graphene and its derivatives have been targeted as the most attractive candidates, as the huge surface area and excellent electrical conductivity of graphene can facilitate both massive accessible active sites and fast charge transfer, thus give rise to high energy and power densities of MSCs [6,7]. Representative examples of reduced graphene oxide (rGO) [8], electrochemically exfoliated graphene (EG) [9], laser-scribed graphene (LSG) [10] as well as their pseudocapacitive compounds, such as rGO/Fe_2O_3 [11], LSG/MnO_2 [12] and EG/polyaniline [13], have been intensively studied to build MSCs that demonstrated long-term cyclability and fast power delivery. However, some of their performance are still far from the optimum to practically power the client micro-devices due to the issues of faint electrostatic double layer charge (EDLC) storage or strong graphene layer restacking with sharply declined effective surface area of charge accumulation [14]. More importantly, these devices are primarily constructed based on non-standard microfabrication process, which cannot be easily transferred into the mature silicon-based process flow and set great difficulties to further progress system-level integration with other electronics [5]. Graphene nanowall (GNW) emerged as a new alternative since its unique feature of spatially aligned graphene network providing a more stable morphology with large surface area up to 1500 $m^2 g^{-1}$. Its open sharp edge has been recognized as an ideal conductive scaffold for supporting pseudocapacitive materials to favor ions diffusion with low energy barriers in a redox system, thus benefits better capacitive behavior [15,16]. Nevertheless, fabricating GNW-based chip-scale pseudocapacitor by harnessing the existed semiconductor process flow has rarely been investigated.

In addition, another strategy to improve the properties and leap forward practical application of MSCs relies on the device architectures evolution. Previously, a great deal of attention has been focused on the planar MSCs configuration, for which electrode materials are surface-mounted on substrates [17]. However, this leaves the bulk of substrates with vast un-used volume and exposes entire fragile electrode nanostructures, which will be easily destroyed during further device encapsulation [18]. On the contrary, fabricating a 3D electrode structure [19] by leveraging the bulk substrate thickness to generate additional surfaces of the sidewall and bury electrode nanomaterials inside the substrate not only allow more active materials to be loaded at footprint with areal capacitance enhancement, but also favors protecting electrode nanostructures.

In this paper, a novel solid-state MSCs based on 3D hierarchical electrodes was developed through fully MEMS-compatible processes by depositing GNW/ruthenium oxides (RuO_x) hybrid nanostructures on the spiral silicon microstructures that generated from deep reactive ion etching (DRIE). In particular, a reactive sputtering is employed for direct thin-film deposition of RuO_x on individual GNW nanoflakes, which allows better coating uniformity than that of the commonly used electrodeposition method and gives possibilities for a fast fab-level processing. In addition to merge the merits of the huge active surface area and the excellent electrochemical behaviors of the GNW/RuO_x hybrid at nanoscale, an in-chip design was utilized by leveraging the sidewall of the DRIE-organized Si microstructures to provide further increased specific area at footprint for areal performance augmentation. While this hierarchical hybrid electrode results in high areal energy, power densities and excellent cycling stability of the as-fabricated MSCs, the unique in-chip device architecture also provides a novel strategy to ease the device encapsulation by embedding the electrode nanomaterials inside the substrate with reduced damage risk.

2. Experimental

2.1. The synthesis of GNW

The growth of GNW on arbitrary substrates, such as Si, was performed through the microwave plasma-enhanced chemical vapor deposition (MPECVD, Seki-AX5200S) with the gas reactants of H_2 and CH_4, as we reported previously [20]. Briefly, the substrate was exposed to 700 W plasma for 10 min pre-treatment under 50 sccm flow rate of H_2. Afterwards, 10 sccm flow rate of CH_4 was introduced to initiate the GNW growth. During the whole deposition, the chamber pressure was remained at 4000 Pa. After deposition, the plasma and gas flow were switched off and followed by 2 h natural cooling.

2.2. Microfabrication process of the in-chip 3D MSCs

The typical fabrication process flow of the 3D MSCs are illustrated in Fig. 1(b). (i) Heavily doped N-type Si wafer (300 μm-thick, 0.01–0.03 Ω cm) was etched through into a couple of inter-digitated Archimedean spiral electrodes via the DRIE method. The electrodes were kept as an integrity of monolithic structures by a pair of connections. (ii) GNW was grown on the as-fabricated Si microstructures via the MPECVD method for 20 min deposition. (iii) The as-deposited GNW was then coated with 150 nm-thick RuO_x using a reactive sputtering technique at the presence of oxygen and argon atmosphere, which was denoted as the 3D GNW/RuO_x-1 for a further comparison, as it will be discussed later. Sputtering from both top and bottom sides of the Si substrate were performed to compensate the non-uniform RuO_x coating at the sidewall of electrode finger, as considering the much lower deposition rate in the deep trenches than that of top surface. (iv) The as-obtained hybrid electrode was then bonded onto a glass wafer with SU-8 dry-film photoresist. (v) The MSCs device was finally released by removing the connections with YAG-laser cutting.

To enable a solid-state 3D MSCs device, the H_3PO_4/polyvinyl alcohol (PVA, Mw ~ 125000, Sigma-Aldrich Co. LLC.) gel was utilized as the electrolyte in this work. The gel electrolyte was prepared by dissolving PVA (1 g) into 30 mL deionized water and mixing with 1.5 g of H_3PO_4 (Kanto chemical Co., Inc.) [21]. The mixture was then vigorously stirred at 85 °C for 2 h and naturally cooled down to obtain a clear viscous liquid. The gel was subsequently injected into the electrode area of the MSCs, which followed by repeat evacuation-venting operations in a vacuum chamber to facilitate the electrolyte wetting on the nanostructures inside the DRIE deep trenches. Finally, the MSCs was remained for 6 h drying at ambient condition prior to the measurements.

2.3. Materials and device characterizations

The electrode materials and the device are routinely characterized using a field-emission scanning electron microscopy (Hitachi SU70, FE-SEM) equipped with energy-dispersive X-ray spectroscopy (EDX). Raman measurement was performed in a NRS-5100 (JASCO Inc., Tokyo, Japan) spectrometer with a 532 nm wavelength incident laser and a 100 × objective with ~1 μm laser spot size.

2.4. Electrochemical measurements

The electrochemical performance of the electrodes and the solid-state MSCs device were evaluated through a cyclic voltammetry (CV) and galvanostatic charge-discharge (GCD) measurements with an electrochemical workstation (Hokuto HZ-7000). The hierarchical hybrid electrode was tested via a three-electrode configuration in