Optics Communications 431 (2019) 58–62

Contents lists available at ScienceDirect

Optics Communications

journal homepage: www.elsevier.com/locate/optcom

Demonstration of an on-chip broadband polarization splitter and rotator using counter-tapered coupler

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A R T I C L E I N F O

Keywords:
Integrated optics devices
Polarization engineering
Silicon on insulator

A B S T R A C T

A broadband and fabrication-tolerant polarization splitter and rotator (PSR) using a counter-tapered coupler is proposed and demonstrated on silicon-on-insulator (SOI) platform. Compared to previously reported PSRs based on a conventional directional coupler, which suffer from relatively low bandwidth and stringent fabrication requirements, the introduced counter-tapered structure can be used to enlarge the bandwidth and fabrication tolerance. The proposed PSR can be fabricated through a single step of lithography and etching, with a total length of 170 μm. The measured results show that the fundamental transverse magnetic (TM_0) to fundamental transverse electric (TE_0) polarization conversion loss is less than 0.8 dB, while the TE_0-TE_0 insertion loss is less than 0.5 dB, over the wavelength range from 1520 to 1580 nm. The polarization crosstalk is lower than -20/-18 dB for TE_0/TM_0 mode, respectively.

1. Introduction

Silicon photonics has been regarded as a promising platform for large-scale photonic integration because of the high refractive index contrast and resulting compact footprint [1]. However, the strong birefringence, introduced by the high refractive index contrast, makes the silicon-on-insulator (SOI) devices polarization-dependent. A common solution for this is using the polarization diversity scheme consisting of polarization beam splitters (PBSs) [2,3] and polarization rotators (PRs) [4,5]. In 2011, a novel concept of polarization splitter and rotator (PSR) was proposed to carry out both polarization splitting and rotation in a single device consisting of an adiabatic taper and an asymmetric directional coupler (ADC) [6]. The operation principle is based on mode hybridization. This type of PSR consists of a TM_0 to first order transverse electric (TE_1) polarization rotator and a TE_1 to fundamental transverse electric (TE_0) mode converter in series. Some similar designs were proposed with bi-level taper for the TM_0-TE_1 polarization rotation [7,8] and an asymmetric Y-branch [9] or a multimode interference coupler [10,11] for mode conversion. Although this kind of device usually has a low crosstalk, a wide bandwidth and a large fabrication tolerance, the footprint is large owing to the two cascaded parts. The other principle for PSR is based on phase matching condition. In the case, a high-efficient cross-polarization coupling occurs once the condition is satisfied. A typical structure for this type of PSR is an ADC which couples a narrow and a wide silicon waveguide [12]. Although the devices based on this principle are usually compact, they are generally wavelength-sensitive and have stringent fabrication requirements. In order to improve the bandwidth or fabrication tolerance for this type of PSR, some modified designs have been proposed. In [13], Ding. et al. proposed a fabrication tolerant PSR based on a tapered directional coupler consisting of a straight narrow waveguide and a linearly tapered one. Nevertheless, that PSR outputs two fundamental transverse magnetic (TM_0) modes and cannot be connected with common used TE_0-input devices. In addition, subwavelength grating [14,15] and partially-etched coupler [16,17] were also introduced to enhance the PSR performance. From the reported schemes, it can be found that there is still a demand for realizing a PSR with both high performance and relatively compact footprint. In recent years, some great theoretical works have been done to reach the goal, but no experiments were carried out [18–20].

In this paper, we propose and experimentally demonstrate an on-chip PSR using a counter-tapered coupler. Air-cladded SOI waveguides are employed to break the vertical symmetry, realizing a strong cross-polarization coupling. Benefitting from the proposed counter-tapered structure, the coupling between TM_0 and TE_0 modes is approximately adiabatic, ensuring that the device has both large bandwidth and small footprint. The measured TE_0-TE_0 insertion loss is less than 0.5 dB and the TM_0-TE_0 polarization conversion loss is less than 0.8 dB over a bandwidth of 60 nm. The polarization crosstalk is lower than -20/-18 dB for TE_0/TM_0 mode, respectively. The proposed design provides a new solution to achieve a high performance PSR with relatively compact structure and simple fabrication process.

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https://doi.org/10.1016/j.optcom.2018.09.015
Received 16 June 2018; Received in revised form 23 August 2018; Accepted 7 September 2018
Available online xxxx

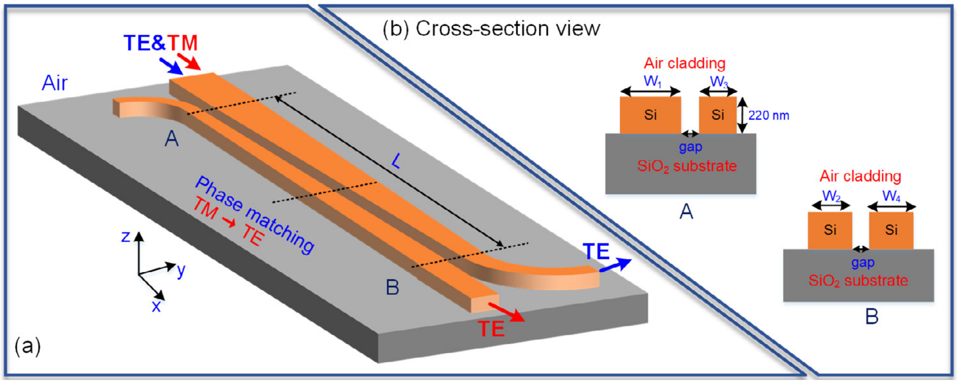

Fig. 1. The schematic configuration and the geometric parameters of the proposed PSR. (a) The three-dimensional schematic of the PSR. (b) The cross-section views of A and B.

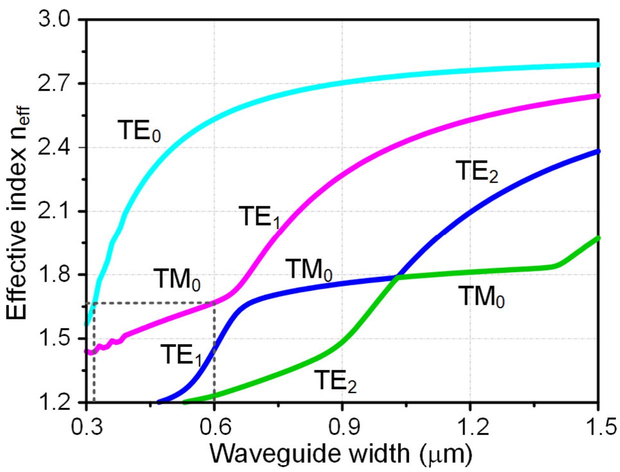

Fig. 2. The calculated effective indices for the eigenmodes of SOI waveguide with air upper cladding.

2. Design principle and simulation

The proposed PSR is designed and fabricated on 220 nm SOI wafer. Fig. 1(a) illustrates the three-dimensional schematic of the device, which consists of two tapered waveguides. The cross sections of points A and B are shown in Fig. 1(b). The width of WG1 is tapered from w1 to w2, while that of WG2 is from w3 to w4. We assume that $w1 - w2 = w4 - w3$, and thus the gap between the two waveguides is constant. The coupling length L is defined as the length of the coupling region. The vertical asymmetry is realized by using air cladding, and a high cross-polarization coupling efficiency can be achieved if the phase matching condition is further satisfied.

The operation principle is based on mode evolution and phase matching. By appropriately choosing the waveguide widths, the phase matching condition can be satisfied, which means the effective index of TM_0 mode in WG1 is equal to that of TE_0 mode in WG2. Therefore, the input TM_0 mode can be efficiently coupled to TE_0 mode in the cross waveguide if the coupling length L is large enough. On the other hand, there is a significant effective index mismatch between TE_0 modes in the two waveguides, resulting in that the input TE_0 mode propagates straightly to the through port and thus the crosstalk at the cross port is very low. The gap between the two waveguides is 200 nm, which is the typical size for easy fabrication. We calculate the effective index of an air-cladded SOI waveguide as a function of the width varied from 0.3 to 1.5 μm at 1550 nm. From Fig. 2, one can deduce that the phase matching condition is satisfied at the position of L/2, where the widths of the two waveguides are 0.6 μm and 0.32 μm. The width of WG1 is tapered from 0.63 to 0.57 μm, while the one of WG2 is from 0.29 to 0.35 μm. The input TM_0 mode will be converted to TE_0 mode around the phase matching point. Beyond this region, the converted mode will not be coupled back owing to the large difference between the effective indices of the two modes. The phase matching points are slightly different for various wavelengths. However, they can always be found along the coupling region. Thus, a high-efficient coupling with small power exchange will be observed for all the wavelengths. Generally, large width difference of the tapered waveguides enlarges the bandwidth, at the cost of increasing the coupling length. In addition, properly decreasing the gap distance can shorten the coupling length while lower the fabrication tolerance.

We use the three-dimensional finite difference time domain (3D-FDTD) method to simulate the proposed PSR. Fig. 3(a) shows the conversion efficiency of TM_0 to TE_0 mode at 1550 nm. The results indicate that the coupling efficiency increases with the increasement of coupling length L, and it is higher than 95% when L is longer than 150 μm. Therefore, $L = 170$ μm is chosen to make a compromise between performance and device footprint. For now, all the parameters of the PSR are determined and the simulated distributions of electric field intensity along the propagation distance are shown in Fig. 3(b) and 3(c). The insets show the cross-section views of mode distribution at three typical sections. The input TE_0 mode stays in WG1 along the coupling region with negligible power being coupled to WG2, and it finally outputs from the through port. By contrast, the TM_0 mode is gradually coupled to the adjacent waveguide and then it is converted to TE_0 mode at the cross port.

Benefitting from the counter-tapered structure, the bandwidth of the designed PSR can be enlarged. For TE_0 mode inputting, the insertion loss is defined as the power ratio of output TE_0 mode at through port to the input TE_0 mode. For TM_0 mode inputting, the loss is defined as the polarization conversion efficiency from TM_0 to TE_0, namely the power ratio of output TE_0 at cross port to the input TM_0 mode. The simulated losses are shown in Fig. 4(a). The TE_0–TE_0 insertion loss can be neglected from 1500 to 1600 nm, while the TM_0–TE_0 polarization conversion loss is less than 0.4 dB. Another key parameter of a PSR is the crosstalk, which is defined as the power ratio of TE_0 mode at untargeted output port to the targeted one, namely,

$$\begin{aligned} XT_{TE-input} &= 10\log\left(P_{TE}^{cross}/P_{TE}^{thru}\right) \\ XT_{TM-input} &= 10\log\left(P_{TE}^{thru}/P_{TE}^{cross}\right) \end{aligned} \quad (1)$$

The mode expansion method is utilized to analyze the crosstalk, as shown in Fig. 4(b). The crosstalk is lower than −25 dB over the wavelength of interest.

To investigate the fabrication tolerance, we sweep the geometry parameters (w1, w2, w3, w4 and gap) of the PSR. Here, w1, w2, w3 and w4 vary with a same value Δw and the gap varies correspondingly to keep the center-to-center waveguide distance constant. As shown in Fig. 5, the tolerance to the deviation of waveguide width is better than 30 nm, on the condition that the conversion efficiency is higher than −1 dB. The improved tolerance of the proposed device attributes to the fact that the width deviation does not break the phase matching condition but only affects the point of phase matching.