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Thin reduced graphene oxide interlayer with a conjugated block copolymer for high performance non-volatile ferroelectric polymer memory

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ABSTRACT

Polymer ferroelectric-gate field effect transistors (Fe-FETs) employing ferroelectric polymer thin films as gate insulators are highly attractive as a next-generation non-volatile memory. For minimizing gate leakage current of a device which arises from electrically defective ferroelectric polymer layer in particular at low operation voltage, the materials design of interlayers between the ferroelectric insulator and gate electrode is essential. Here, we introduce a new solution-processed interlayer of conductive reduced graphene oxides (rGOs) modified with a conjugated block copolymer, poly(styrene-*block*-paraphenylene) (PS-*b*-PPP). A FeFET with a solution-processed p-type oligomeric semiconducting channel and ferroelectric poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) insulator exhibited characteristic source–drain current hysteresis arising from ferroelectric polarization switching of a PVDF-TrFE insulator. Our PS-*b*-PPP modified rGOs (PMrGOs) with conductive moieties embedded in insulating polymer matrix not only significantly reduced the gate leakage current but also efficiently lowered operation voltage of the device. In consequence, the device showed large memory gate voltage window and high ON/OFF source–drain current ratio with excellent data retention and read/write cycle endurance. Furthermore, our PMrGOs interlayers were successfully employed to FeFETs fabricated on mechanically flexible substrates with promising non-volatile memory performance under repetitive bending deformation.

1. Introduction

Ferroelectric-gate field effect transistors (Fe-FETs) with ferroelectric polymer gate insulators have drawn great attraction due to their low production cost, non-destructive memory operation through semi-conducting channel, scalable feature size of $4F^2$, low operating voltage and the potential for use in flexible devices of interest in many emerging mobile applications [1–5]. The representative ferroelectric polymers include poly(vinylidene fluoride) (PVDF) and its copolymers with trifluoroethylene (TrFE) (PVDF-TrFE) in which ferroelectric switching is accompanied by facile rotation of the bistable permanent dipole between hydrogen and fluorine atoms along the polymer chain upon altering the polarity of an electric field [6]. Since

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the concept of FeFETs with ferroelectric polymers have been introduced [7,8] significant progresses in memory performance of Fe-FETs have been made by addressing various scientific and technical issues including nondestructive readout capability [5,9,10], scalability, flexibility [11–13], printing capability [9,14], endurance [5,15], long data retention [4,5,9], short program pulse width [5], large ON/OFF ratio [4,5,9,10,14] and materials design including electrodes [5], ferroelectric and insulating layers [4,9,16] and semiconducting active channel layers [4,5,9,10,14,17–25].

In spite of the great advance in FeFET performance, there are still technological as well as scientific issues to be addressed for the better understanding of device operation and thus realization of high performance non-volatile memory. One of the most critical issues is the appropriate design of interfaces of ferroelectric gate insulator with either gate electrode or semiconducting channel. Since the charge injection from semiconductor to ferroelectric layer rarely occurred due to the high energy band gap of most ferroelectric polymers in organic Fe-FETs [2], the majority of the previous works have been focused on the interface between metal and PVDF-TrFE for minimizing contamination of a ferroelectric layer by diffusion of metal atoms upon deposition in metal/ferroelectric/metal capacitors [3,26,27] and for developing effective ferroelectric crystal orientation on metal surface modified with self assembled monolayers [28]. In addition, tremendous efforts have been also made for reducing the gate leakage current of a ferroelectric layer which results from many structural defects arising from grain boundaries of semicrystalline polymers, pinholes and residual solvent trapped in the film [17,19]. This issue became more important in particular when designing a low voltage operation FeFET with a very thin ferroelectric insulator. A reduction in ferroelectric film thickness due to its high coercive field of approximately 50 MV/m is often accompanied by a decrease in polarization level and an increase in switching time, mainly attributed to the decrease of the degree of crystallization [27,29–32]. In addition, thin PVDF-TrFE films become structurally non-uniform, giving rise to high leakage current. It is, therefore, a great challenge to develop a route to minimize gate leakage current of a FeFET that operates at a voltage as low as possible with high reliability of the stored data.

A variety of interlayers have been employed, including SiO_2 [21,33], Al_2O_3 [23,24,34], PVP [4,9,35], and random copolymer of polystyrene and poly(methylmethacrylate) (P(S-*r*-MMA)) [17] with the general design rule that makes an uniform interlayer as thin as possible while keeping high capacitance. Additional benefits of polymeric interlayers such as cost effective fabrication based on solution processes and interfacial compatibility with ferroelectric polymer have made them very attractive for the purpose. Alternatively to overcome the issue of relatively low dielectric constants of majority of polymers which frequently resulted in very high device operation voltage, conducting polymer interlayers have been proposed in the architecture of metal/ferroelectric/metal (MFM) capacitors such as poly(3,4-ethylene dioxythiophene) (PEDOT) [26,30,36,37], polypyrrole [10,27] and polyaniline (PANI) [38]. For instance, the improved fatigue property of MFM capacitors was obtained with an ultra-thin (ca. 50 nm) PEDOT–PSSH interlayer between bottom electrode and ferroelectric layer [26]. The poor environmental stability of the conductive polymers may, however, limit their use of interfacial layers for practical applications.

Conductive reduced graphene oxide (rGO) nanosheets, mechanically flexible two dimensional sheets of sp^2 hybridized carbon atoms, can be a good candidate as an interlayer for high performance FeFETs when properly processed for fabricating thin uniform films inserted between ferroelectric and metal layer. We envisioned that a thin composite film of rGOs with a conjugated block copolymer, poly(styrene-*block*-paraphenylene) (PS-*b*-PPP), which we have recently developed [39] could be suitable as an interlayer. Solution-processed PS-*b*-PPP modified rGOs (PMrGO) layers consist of conductive rGOs embedded in an insulating PS-*b*-PPP in which conjugated PPP block strongly adhere to the rGO surface because of its isomorphic molecular skeleton to the honeycomb structure present on the graphene surface, while the PS block offers good insulating medium.

In this work, we present non-volatile ferroelectric memory performance of bottom gate top contact FeFETs containing PMrGO interlayers. A FeFET with a solution-processed p-type oligomeric semiconducting channel of dicyanomethylene-substituted quinoidal quaterthiophene (QQT(CN)4) exhibited characteristic source–drain current hysteresis arising from ferroelectric polarization switching of a PVDF-TrFE insulator [11]. Systematic investigation of FeFETs with composite interlayers containing two different concentrations of rGOs revealed that introduction of PMrGO layer between gate electrode and PVDF-TrFE layer not only significantly reduced the gate leakage current but also lowered the operation voltage. High yield FeFET devices successfully operated at gate voltage sweep of ±25 V with fully saturated current hysteresis having high ON/OFF ratio and excellent data retention and read/write cycle endurance while the similar performance was obtained at ±50 V without an interlayer. Furthermore, our PMrGOs interlayers are successfully employed to FeFETs fabricated on mechanically flexible substrates with promising non-volatile memory performance under repetitive bending deformation.

2. Experimental

2.1. Materials

Graphite powder (<45 μM), $KMnO_4$, H_2O_2, H_2SO_4, HCl, acetone, chloroform, N,N′-dimethylformamide (DMF), methanol, methyl ethyl ketone (MEK), tetrahydrofuran (THF) and toluene were purchased from Sigma–Aldrich and used as received unless otherwise stated. Poly(styrene-*block*-paraphenylene) with polyphenylene rich in 1,4-addition (PS-*b*-PPP) was procured from Polymer Source Inc., Doval, Canada. The molecular weights of the PS and PPP are 4800 g mol^{-1} and 1100 g mol^{-1}, respectively. The polydispersity index (PDI) of the PS-*b*-PPP is 1.10. P(VDF-TrFE) copolymer (with 25 wt% TrFE) used in this study was purchased from MSI Sensor, PA. The melting and Curie temperatures of the P(VDF-TrFE) copolymer are (T_m) ~150