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Low operational voltage and high performance organic field effect memory transistor with solution processed graphene oxide charge storage media

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ABSTRACT

Low voltage organic field effect memory transistors are demonstrated by adapting a hybrid gate dielectric and a solution processed graphene oxide charge trap layer. The hybrid gate dielectric is composed of aluminum oxide (AlO_x) and [8-(11-phenoxy-undecyloxy)-octyl]phosphonic acid (PhO-19-PA) plays an important role of both preventing leakage current from gate electrode and providing an appropriate surface energy to allow for uniform spin-casting of graphene oxide (GO). The hybrid gate dielectric has a breakdown voltage greater than 6 V and capacitance of 0.47 μF/cm^2. Graphene oxide charge trap layer is spin-cast on top of the hybrid dielectric and has a resulting thickness of approximately 9 nm. The final device structure is Au/Pentacene/PMMA/GO/PhO-19-PA/AlO_x/Al. The memory transistors clearly showed a large hysteresis with a memory window of around 2 V under an applied gate bias from 4 V to −5 V. The stored charge within the graphene oxide charge trap layer was measured to be 2.9×10^{12} cm^{-2}. The low voltage memory transistor operated well under constant applied gate voltage and time with varying programming times (pulse duration) and voltage pulses (pulse amplitude). In addition, the drain current (I_{ds}) after programming and erasing remained in their pristine state after 10^4 s and are expected to be retained for more than one year.

1. Introduction

Since curved smart phones based on organic light emitting diodes (OLEDs) have commercialized, organic based electronic components such as light emitting diodes, photovoltaics, memory, and transistors have been spotlighted due to their potential use in flexible electronics [1–5]. Organic transistors have received significant attention from both academia and corporate interests due to their fundamental capability to act as a basic switching unit, a basic component of integrated circuits. Additionally, it may be cost-advantageous to integrate organic transistors with OLEDs rather than the more traditionally used inorganic amorphous silicon transistors. Utilizing organic transistors to control the backplane of an OLED display is

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just one potential application of organic electronic circuitry. Another use of organic transistors for electronic circuits is a memory transistor which contains both a memory and switching element and has been widely pursued for potential applications in data storage [6]. Recently, areas of research for organic memory transistors are mostly focused on charge storage media such as polymer electrets, metal nanoparticles, metallic thin-films, 2-dimentional nanomaterials and ferroelectric polymers [7–17]. Furthermore, low voltage operation, utilization of solution processable materials, and a cost effective charge trap layer are important for practical realization of printable organic memory devices.

In order to achieve low voltage organic memory transistors an appropriate dielectric and charge trapping layer need to be selected. The operational voltage of an organic transistor can be modulated by controlling the total dielectric thickness (d) and dielectric constant (k). Research into low voltage platforms for organic transistors is varied and several suitable dielectric systems such as high-k transition metal oxides (TMO), ion-gels, and hybrid systems using a stacked self-assembled monolayer (SAM) and an ultrathin high-k TMO layer have been studied [18–23]. In particular, hybrid gate dielectrics have exhibited excellent dielectric properties due to both high accumulation of charges on the dielectric surface and the ability to control the surface energy via a SAM which enables the use of solution processed organic semiconductors. Additionally, the SAM serves to screen the relatively unstable charge distribution of the high-k TMO. The molecular structure of SAMs can also be designed to have less leakage current and higher or lower surface energy by adjusting length of molecule and end functional groups. Due to these properties, hybrid dielectrics are a promising platform for low voltage organic memory transistors. Another important component for organic memory transistor is the charge-trapping layer which is generally employed between the gate and tunneling dielectric layers. From a processability and cost-efficiency point of view, graphene oxide an exemplary candidate for next generation charge trapping layers in organic memory transistors. Key advantages of graphene oxide is that it is well dispersed in water-based solvents and has many charge trapping sites due to structural defects and the presence of hydroxyl and carboxyl groups [24,25].

In order to demonstrate solution processed low voltage organic memory transistors, we used a hybrid gate dielectric composed of aluminum oxide (AlO_x) and [8-(11-phenoxy-undecyloxy)-octyl]phosphonic acid (PhO-19-PA) SAM. The surface energy of the phenoxy end group of the PhO-19-PA SAM enables the spin-casting of the graphene oxide charge trap layer. The final device structure was Au/Pentacene/PMMA/GO/PhO-19-PA/AlO_x/Al. The memory transistors showed a large hysteresis with a memory window of around 2 V under an applied gate bias from 4 V to −5 V. The stored charge within the graphene oxide charge trap layer was measured to be 2.9×10^{12} cm^{-2}. The low voltage memory transistor operated well under constant applied gate voltage and time with varying programming times (pulse duration) and voltage pulses (pulse height). In addition, the threshold voltage after programming and erasing remained in their pristine state after 10^4 s and are expected to be of use for more than one year.

2. Experimental details

Heavily doped n-type silicon substrates were first cleaned in piranha solution which is a mixture of sulphuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2) (3:1 by volume) at 70 °C for 10 min. After rinsing with de-ionized (DI) water, ultrasonication was performed for 10 min in a mixture of DI water (H_2O), ammonium hydroxide (NH_4OH), and hydrogen peroxide (H_2O_2) (5:1:1 by volume). The substrates were rinsed again in DI water and dried with nitrogen gas. A 30 nm thick aluminum gate electrode

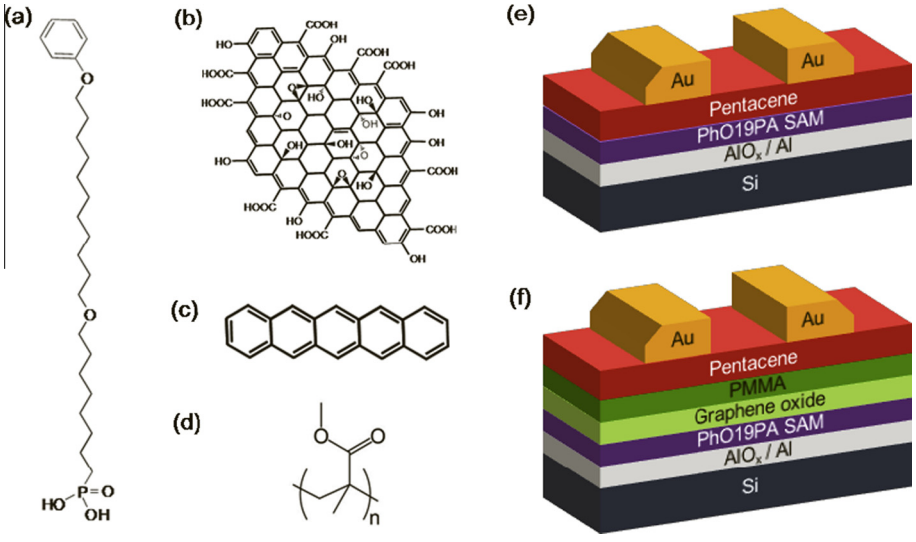

Fig. 1. Chemical structures of (a) [8-(11-phenoxy-undecyloxy)-octyl]phosphonic acid (PhO-19-PA), (b) graphene oxide sheets prepared by a modified Hummer's method, (c) pentacene and (d) poly(methylmethacrylate) (PMMA). Device structures of (e) reference transistor and (f) memory transistor.