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Letter

The mutual influence of surface energy and substrate temperature on the saturation mobility in organic semiconductors

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ABSTRACT

We report on a mutual correlation between the substrate temperature during semiconductor deposition and the surface energy of the gate dielectric on the charge carrier mobility in bottom gate top contact organic field effect transistors (OFETs) with N,N′-diphenyl-3,4,9,10-perylene tetracarboxylic diimide (DP-PDI) as organic semiconductor.

The gate dielectric consists of a thin gate aluminum oxide and a self-assembled monolayer (SAM) with which the surface energy of the hybrid dielectric is tuned. The substrate temperature during evaporation of the DP-PDI semiconductor was systematically varied to obtain the best charge carrier mobility for each SAM. We found that the optimum substrate temperature correlates with the surface energy. Devices with low surface energy reach best mobility at higher substrate temperatures than devices with a higher surface energy.

1. Introduction

The interest in OFETs has rapidly increased in recent years, due to their potentially inexpensive and simple processing and the possibility to use them in new applications such as flexible electronics [1]. Electrical performances and especially charge carrier mobilities have been improved in recent years by introducing new molecular structures for organic semiconductors (SCs) [1–5]. Additionally, many efforts have been taken to control the morphology of the organic SC as one of the key aspects that determines the electrical performance in particular [6–10]. Improvements have been achieved in controlling the molecular orientation at the dielectric-semiconductor interface by optimized deposition and post treatment steps [11–13] and/or tuning the dielectric surface with SAMs. With a hybrid dielectric, consisting of a thin gate oxide and a SAM on top, high capacitances can be achieved, which leads to low-voltage operation with simultaneously low gate leakage currents [14]. Moreover, the SAM as dielectric surface can influence the growth of the SC molecules [6,10]. By varying the chemical structure of the SAM molecules, in particular at the head group, a change in surface energy (SE) of the hybrid dielectric can be achieved, providing a surface for the semiconductor deposition with desired SE. Although several studies have addressed the influence of process parameters such as substrate temperature or surface treatment to control the semiconductor growth [6–9,15,16], to our knowledge there are no investigations in which the mutual influence of both parameters is correlated to the electronic properties in transistor devices.

Here we present a correlation between the SE, varied by different SAMs, and the optimum substrate temperature during SC evaporation for the electrical performance of organic thin film transistors with DP-PDI as the active, semiconducting molecule. With knowledge of this correlation it is possible to assess the favorable substrate temperature for SC evaporation, if the surface energy of

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the dielectric is known. The molecular structures of the self-assembling molecules as well as the DP-PDI and the structural setup of a bottom-gate top-contact OFET are shown in Fig. 1.

2. Experimental

All chemicals were used as received, without further purification, from Sigma Aldrich (N,N′-diphenyl-3,4,9,10-perylene tetracarboxylic diimide (DP-PDI) and 16-phosphonohexadecanoic acid (PHDA)), Sikemia (Heptadecafluorodecylphosphonic acid ($F_{17}C_{10}$-PA), 10-Undecynylphosphonic acid (HCC_9-PA) and (12-chlorododecyl)phosphonic acid (ClC_{12}-PA)), Dr. Schlörholz (pentadecafluorooctadecylphosphonic acid ($F_{15}C_{18}$-PA)) and PCI Synthesis (tetradecylphosphonic acid (C_{14}-PA)).

2.1. Device fabrication

Bottom-gate top-contact transistors were fabricated according to standard procedures [17]. 30 nm aluminum were evaporated through shadow masks onto a silicon-wafer with 100 nm SiO_2 (pressure below 10^{-6} mbar, evaporation rate approx. 2.0 Å/s) to form gate electrodes. An oxygen plasma treatment was performed in a plasma chamber (Electronic Diener Plasma-Surface-Technology) with an O_2-preassure of 0.2 mbar for 5 min to generate a thin and dense aluminum oxide AlO_x-layer of approximately 3.6 nm thickness [17]. Monolayers of phosphonic acids were self-assembled from solution (0.2 mM in 2-propanol, immersion time between 24 h and 72 h). Afterwards the samples were rinsed with pure 2-propanol, dried in a stream of nitrogen and on a hot plate (60 °C, 3 min) [18]. DP-PDI was evaporated through shadow masks as active layer with a thickness of 30 nm (pressures below 4×10^{-6} mbar, evaporation rate approx. 0.1 Å/s). During semiconductor evaporation the substrate temperature ($T_{substrate}$) was kept constant at temperatures between 60 °C and 140 °C. Finally, gold source and drain structures were evaporated through shadow masks (thickness: 30 nm, evaporation rate: 1.0 Å/s, pressures below 3×10^{-5} mbar). The fabricated devices exhibit a channel length of 40 μm and a channel width of 600 μm.

2.2. Contact angle and surface energy measurement

For contact angle and surface energy measurements of the SAMs, silicon wafers with 30 nm evaporated and oxygen plasma treated aluminum served as substrate for the self-assembly. The contact angles of the SAM covered substrates to water, formamide and diiodomethane (droplet volume: 2 μl) were measured with the sessile drop method on an OCA-2.0 contact angle measurement device (DataPhysics Instruments GmbH). From these contact angle values surface energies were calculated using the method of Owens, Wendt, Kaelble and Rabel employing values for the surface energies of the fluids from Busscher et al. [19,20].

2.3. Electrical characterization

Capacitance measurements were realized by an Agilent B1500A parameter analyzer. The capacitance was measured at a frequency of 500 kHz and a voltage of 1 V and normalized to the area. Transistors were characterized with an Agilent 4156C parameter analyzer unit in a glove box with nitrogen atmosphere. Output and transfer characteristics of at least 4 transistors for each SAM and substrate temperature were measured with drain and gate voltages in the range of −1 V to 3.5 V. Charge carrier mobilities in linear and saturation mode, threshold voltages, on/off-ratios and I_D/I_G-ratios were extracted from the characteristics [1].

2.4. AFM studies

Samples for AFM studies were fabricated on smooth silicon substrates with a 10 nm thin AlO_x layer, grown by atomic layer deposition (ALD). These ALD grown AlO_x

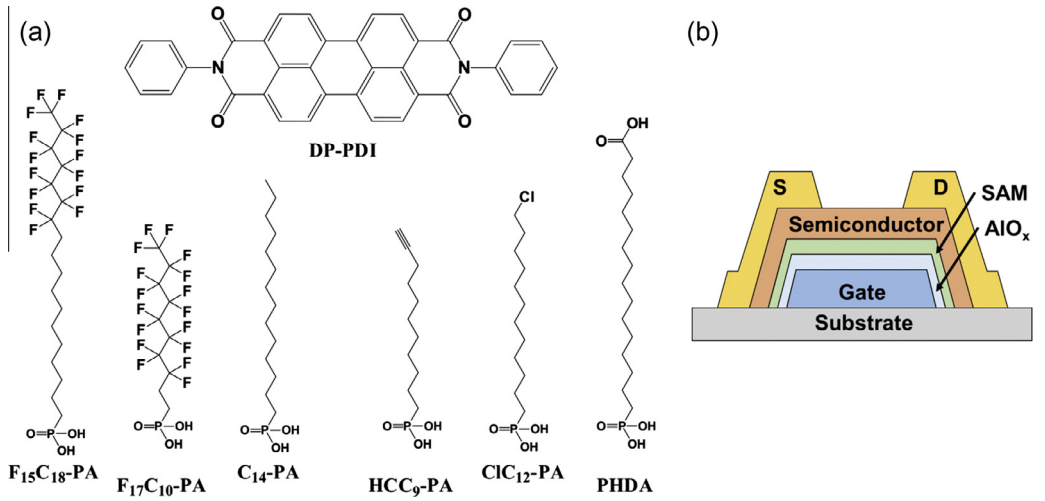

Fig. 1. (a) Structure of the semiconductor N,N′-diphenyl-3,4,9,10-perylene tetracarboxylic diimide (DP-PDI) and the SAM molecules $F_{15}C_{18}$-PA, $F_{17}C_{10}$-PA, C_{14}-PA, HCC_9-PA, ClC_{12}-PA and PHDA. (b) Schematic setup of a bottom-gate top-contact OFET with a hybrid dielectric consisting of a SAM and a thin AlO_x layer.