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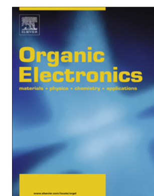

Scaling limits of organic digital circuits

Anita Risteska [a], Kris Myny [b], Sören Steudel [b], Masakazu Nakamura [c], Dietmar Knipp [a,*]

[a] *Research Center for Functional Materials and Nanomolecular Science, Electronic Devices and Nanophotonics Laboratory, Jacobs University Bremen, 28759 Bremen, Germany*
[b] *IMEC, Polymer and Molecular Electronics, Kapeldreef 75, 3001 Leuven, Belgium*
[c] *Graduate School of Materials Science, Nara Institute of Science and Technology, Ikoma, Nara 630-0192, Japan*

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ABSTRACT

The effect of device scaling on organic circuits' performance was studied. Particularly, the influence of contact resistance on the static and the dynamic behavior of the circuits was investigated. For that purpose, an analytical model describing the voltage transfer characteristics (VTCs) and the propagation delay was developed. Using the model, it was shown that for OTFTs with channel lengths of less than 10 μm the contact resistance has negative influence on both, the static noise margin (SNM) and the propagation delay. Moreover, the model is in a good agreement with experimentally measured data. Scaling the lateral dimensions of the transistors down to few μm limits the circuit performance due to contact effects, and the 1–10 MHz frequency range operation required by some applications can only be achieved by reducing the specific contact resistance, ρ_c, 10–100 times. This need for ρ_c reduction highlights the importance of improving charge injection in organic transistors that can usually be achieved by contact doping like in inorganic electronics.

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1. Introduction

Organic thin-film transistors (OTFTs) and organic electronic circuits have been in the focus of intensive research due to their compatibility with low fabrication temperatures, large-area processing and low costs, making them good candidates for the realization of bendable and stretchable electronics. Some of their most important applications include driver circuitry for active-matrix backplanes in displays [1–5] and low cost radio frequency identification (RFID) tags [6,7]. In recent years many efforts have been made to achieve a feasible performance and meet the standards of these technologies in terms of stability [8–10], low voltage operation [11–13], reproducibility [14] and speed [15].

The switching speed of organic transistors and circuits can be increased by scaling down the lateral dimensions of the devices. However, for short channel transistors the performance is limited by contact effects, so that the effective mobility and the speed of the TFTs are reduced and the stage delay of organic digital circuits is increased. Normalized contact resistances ranging from 5 kΩ cm to 10 MΩ cm have been reported for organic and polymeric thin-film transistors [16–20]. These values are high when compared to their inorganic counterparts and have a significant impact on the speed and the drive current of organic TFTs, mainly for transistors with shorter channel length [18].

In the following, the impact of device scaling and contact resistance on the organic circuits' performance will be investigated and discussed through analytical modeling and experiments. The main focus will be on the static and the dynamic behavior of organic CMOS inverters, as the basic building blocks of all digital circuits, and their limitations due to contact effects. Optimal dimensions of the transistors will be derived. Furthermore, strategies to achieve organic digital circuits with high static noise margin and low stage delay will be described.

* Corresponding author.
E-mail address: d.knipp@jacobs-university.de (D. Knipp).

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2. Contact effects in organic thin-film transistors

The contact resistance of organic thin-film transistors is defined by the work function of the materials forming the electrical contact [18]. Furthermore, the contact resistance is determined by the fabrication conditions and the device geometry [21–23]. The resistance of a vertical contact is described by $R_C = \rho_c/A$, where ρ_c is the specific contact resistance and A is the area of the electrical contact. For a lateral contact geometry, the contact resistance of the metal–semiconductor interface can be described by a 2nd order ordinary differential equation [24]. Solving the differential equation leads to the following expression of the normalized contact resistance:

$$r_c = R_C \cdot W = \sqrt{\rho_c \cdot R_{sheet}} \cdot \coth\left(\frac{L_{DS}}{L_T}\right) \tag{1}$$

where R_{sheet} is the sheet resistance of the semiconductor layer, W is the channel/electrode width, and L_{DS} and L_T are the length of the source/drain contacts and the transfer length, respectively as shown in Fig. 1. The transfer length is defined as the distance over which most of the current transfers from the semiconductor into the metal electrodes and vice versa, and is given by:

$$L_T = \sqrt{\frac{\rho_c}{R_{sheet}}} \tag{2}$$

The sheet resistance of the organic layer near the electrodes can be approximated by the channel resistance of the TFT operating in the linear region, for structures with top source/drain electrodes [16]. For transistor structures where the L_{DS} is much larger than the transfer length, the contact resistance can be expressed by $R_C \approx \rho_c/(L_T \cdot W)$. On the other hand, for small and very small contacts, the contact resistance is increased and can be approximated by $R_C \approx \rho_c/(L_{DS} \cdot W)$.

For TFTs with bottom source/drain contacts, the growth of molecules on the conductive electrodes leads to a disordered organic film, while the molecules in the channel of the TFT are highly ordered. As a consequence, the sheet resistance near the source/drain contacts cannot be described by the channel resistance and is given by [16]:

$$R_{sheet\text{-}bottom} = \frac{1}{\mu_c \cdot C_g \cdot (V_G - V_{TH} - V_D/2)} \exp\left(\frac{L_T^2}{L_P^2} \cdot \frac{k \cdot T}{q \cdot V_D}\right) \tag{3}$$

with μ_c being the charge carrier mobility in the contact region, C_g being the gate capacitance per unit area, L_p being the diffusion length of the charge carriers, k is the Boltzmann's constant, T is the absolute temperature, q is the elementary charge and V_G, V_{TH} and V_D are the gate, the threshold and the drain voltage, respectively. If the formation of the organic film is not affected by the drain and source contacts, the charge carrier mobility μ_c is equal to the intrinsic mobility, μ_0.

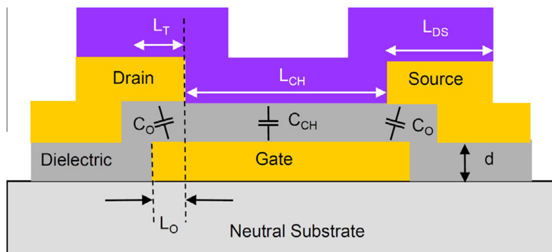

Fig. 1. Cross-section of a bottom-contact coplanar organic thin-film transistor.

The measured normalized contact resistance is plotted as a function of the gate charge per area for different TFT structures in top and bottom contact configuration as shown in Fig. 2(a). The top contact (TC) transistors [21] exhibit 10 times smaller contact resistances than the bottom contact (BC) ones [16,21]. As mentioned before, the reason for this is the alignment of the organic molecules, which has an influence on the electronic structure of the semiconductor. However, these large contact resistances can be reduced by self-assembled monolayer (SAM) treatment of the source/drain electrodes (Fig. 2(a)) [25]. The SAM treatment changes the growth conditions of the organic molecules near the contacts, resulting in an ordered film. This leads to an increase of the lateral conductivity of the organic film (μ_c and L_p increase), which reduces the transfer length and the contact resistance of the bottom source/drain TFT structures. In this case the contact resistance is comparable to that of TC structures (Fig. 2(a) – Myny et al. data). For high drain voltages, the sheet resistance can be approximated by $R_{sheet\text{-}bottom} \approx 1/(\mu_c \cdot C_g \cdot (V_G - V_{TH} - V_D/2))$, which is equivalent to the sheet resistance of TC structures.

Although, TC structures exhibit lower R_C, their minimal channel length is usually limited by the resolution of the fabrication technique, which typically involves shadow masking [21,26,27] and does not allow for aggressive scaling of the transistors down to sub micrometer range. In recent years, few research groups presented top source/drain organic TFTs and circuits with channel lengths down to 5 μm [28,29]. However, the realization of organic transistors and circuits with top source/drain contacts is complex compared to the fabrication of transistors with bottom source/drain contacts. Therefore, in this study we will focus on transistors with bottom-contact geometry, whose cross-section is shown in Fig. 1. As discussed above, the contact resistance can be reduced by SAM treatment and made comparable to that of TC structures (Fig. 2(a)) and the metal contacts can be fabricated by standard photolithography or imprinting [30], allowing for scaling of the channel length (L_{CH}) down to few tens of nanometers.

The drain current of a thin-film transistor operating in the linear region can be described by:

$$I_D = \frac{W}{L_{CH}} \cdot C_g \cdot \mu_{eff} \cdot \left(V_G - V_{TH} - \frac{V_D}{2}\right) \cdot V_D \tag{4}$$

were μ_{eff} defines the device charge carrier mobility including the contact resistance effects and is given by:

$$\mu_{eff} = \frac{L_{CH}}{L_{CH} + r_c \cdot C_g \cdot \mu_0 \cdot \left(V_G - V_{TH} - \frac{V_D}{2}\right)} \cdot \mu_0 \tag{5}$$

Similar equations can be derived for the drain current in the saturation region.

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