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A novel current-mode low-power adjustable wide input range four-quadrant analog multiplier

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ABSTRACT

In this paper, a novel current mode enhanced input range four-quadrant analog multiplier is presented. The proposed class AB based translinear current squarer allows the designer to control the input range via a digital code. Moreover, the proposed scheme improves the linearity of the circuit and has a high robustness against process variations. The Post-layout and Monte Carlo simulations of the multiplier in a 0.18 μm standard CMOS technology show an input range of (1 + m) × 10 μA (where 'm' is an adjustable parameter), a THD of 1% (@ 1 MHz), a −3 dB bandwidth of 332.3 MHz (for m = 3) and a power consumption of 186 μW.

1. Introduction

Real-time analog multiplication of two signals is an important operation in the analog signal processing applications [1]. The multiplier is used in many analog signal processing systems such as modulators and mixers, variable gain amplifiers, adaptive filters, phase locked loops, artificial neural networks and fuzzy logic controllers [1,2].

A significant work for implementing analog multiplication has been conducted in CMOS and BJT mostly focusing on circuit level techniques. Analog voltage mode multipliers, which produce a voltage/current signal proportional to the multiplication of two input voltage signals have been categorized and analyzed in Ref. [1].

However, the voltage mode multipliers undergo various limitations regarding their direct dependence on the voltage supply and sensitivity to process variations. Furthermore, by scaling the technology and consequently scaling the supply voltage, the operating (input) range of this type of multipliers are being squeezed even more.

Current mode signal processing offers low voltage and high speed in comparison to voltage mode signal processing. However, the proposed current mode multipliers thus far, have a limited input range. Based on [3] analog current mode multiplication of two signals is generally realized either in weak inversion or strong inversion. Weak inversion multipliers are an interesting choice for extremely low voltage/power applications; however, they undergo limited input range and narrow bandwidth [4–6].

Various implementations for CMOS current mode strong inversion multipliers have been proposed [7–15]. Fig. 1 shows the block diagram of different realizations of the current mode multiplier in the strong inversion. One approach is to convert the input currents to voltage and then apply the voltage to two/three voltage mode squarers. This technique suffers from strong dependence of the output current to the device parameters and power supply variations [12–15]. Furthermore, the input ranges of these types of multipliers are limited by the maximum allowable voltage swing in the voltage squarer, which is generally limited to the voltage supply. In the second technique, different types of translinear loops (TL) (stacked or up-down configurations [16]) are used to realize the current mode squarer and/or geometric mean blocks as basic building blocks of the multiplier [7–11]. A TL is a special device arrangement that allows a useful large signal relationship among their currents [16–18]. The advantage of this technique over other abovementioned voltage or current mode techniques is in its capability to provide pure current mode output which is independent of device parameter or supply voltage. However, the input range of these types of multipliers is usually limited to the imposed limitation of the current squarer, which is the prerequisite of working in saturation region for all the transistors in the TLs. Moreover, the only way to enlarge input range in these types of multipliers is to increase the bias current, which in turn leads to increase in power.

The proposed multiplier offers a new solution to extend the input range without any increase in the power consumption. This solution combines modified low power class AB current buffer with translinear based current squarer to achieve a wide and adjustable input range multiplier that provides a pure current mode output. It is also shown that this technique improves the linearity of the multiplier. The paper is organized as follows. The proposed circuit is presented in Section 2, the proposed structure is analyzed in section 3, simulation results are

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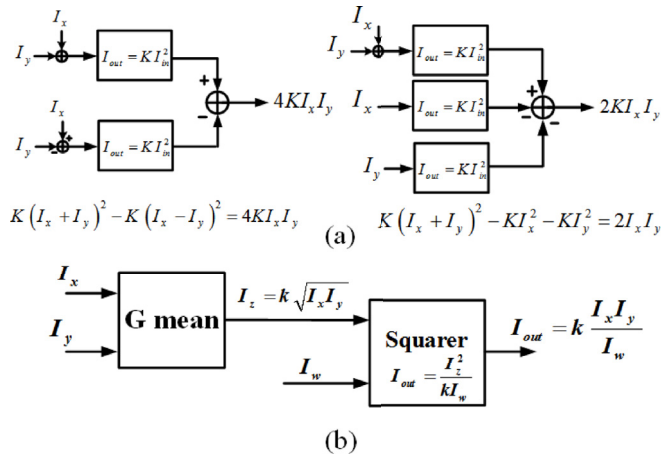

Fig. 1. Block diagram of different realizations of the current mode multiplier in the strong inversion a) Using two/three squarers, b) Using geometric mean-squarer.

shown in Section 4 and conclusions are given in Section 5.

2. Circuit description

The operation of the proposed multiplier is based on the implementation of the quadratic equation as

$$I_{out} = k(I_x + I_y)^2 - k(I_x - I_y)^2 = 4kI_xI_y \tag{1}$$

where I_{out} is the output current, I_x and I_y are input current signals and k is the scaling factor. This technique provides four quadrant operation in principle, while the geometric-mean based technique is only capable of implementing two quadrant multiplication [7]. From (1) it is deduced that two current mode squarers are needed to realize the current mode multiplication. These squarers should provide two quadrant operation in order to achieve four quadrant multiplier. Therefore, the characteristics of the current squarers (e.g. power consumption, input range and linearity) directly determine that of the multiplier.

2.1. Current-mode squarer circuit

The current-mode squarer circuit is shown in Fig. 2. The circuit consists of two sub-blocks which are highlighted in the figure: A modified class AB current buffer stage and a translinear loop formed by $M_1 - M_4$ which are biased in the saturation region [19]. The function of the class AB buffer is to introduce the proper portion of the input current into the TL in such a way that the whole circuit works as a two-quadrant current squaring circuit. The key point is that the input current of the proposed circuit can be two quadrant without any need for extra bias currents thanks to the intrinsic characteristic of the class AB stage. For the sourcing input currents, M11, M17, M9, M7 conveys the current to the translinear loop and for the sinking input currents, M10, M16, M8, M6 do the same. Moreover, it is shown in Section 3.1 that the modified structure of the current buffer helps to extend the input operating range of the squarer beyond the limitation dictated by the

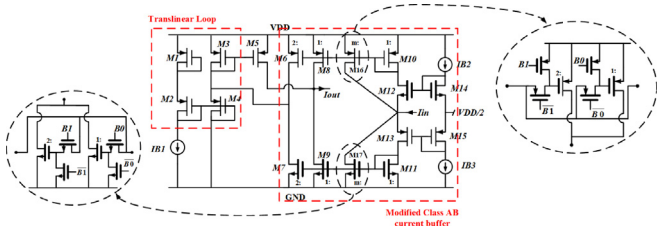

Fig. 2. The proposed Current-mode squarer.

current squarer. Furthermore, it is shown in the following sections that the proposed scheme improves the linearity and robustness of the circuit against process variations. In the circuit the aspect ratios of M_{16} *and* M_{17} (m-transistors) are 'm' times larger than M_{10} *and* M_{11} respectively. Applying KCL in the input node gives:

$$I_{in} = I_{M16} + I_{M10}\ (or:\ I_{in} = I_{M17} + I_{M11}) \tag{2}$$

The currents of transistors M_8 and M_{10} are given as

$$I_{M8} = I_{M10} = \frac{I_{in}}{1+m}\left(or:\ I_{M9} = I_{M11} = \frac{I_{in}}{1+m}\right) \tag{3}$$

Based on the class AB operation, M_8 and M_9 provide two quadrant output current. This is also valid for M_6 and M_7, which their aspect ratios are twice the diode connected transistors M_{10} and M_{11} respectively:

$$I_{M6} = \frac{2I_{in}}{1+m}\left(or:\ I_{M7} = \frac{2I_{in}}{1+m}\right) \tag{4}$$

These currents are injected into the TL in order to realize the two quadrant current squarer. Since the aspect ratios of $M_1 - M_4$ transistors are equal, based on the MOS translinearity (MTL) principle in saturation region ([16])

$$2\sqrt{I_{B1}} = \sqrt{I_{DS3}} + \sqrt{I_{DS4}} \tag{5}$$

where I_{B1} is the bias current of transistors M_1 and M_2. I_{DS3} and I_{DS4} are the drain-source current of transistors M_3 and M_4 respectively, which can be expressed as

$$I_{DS_3} = I_{DS_5} = I_{out} + \frac{I_{in}}{1+m} \tag{6}$$

$$I_{DS_4} = I_{DS_3} - 2\frac{I_{in}}{1+m} = I_{out} - \frac{I_{in}}{1+m} \tag{7}$$

where I_{DS5} is the drain-source current of M_5 and I_{out} is the output current of the squarer. Substituting (6) and (7) into (5) yields

$$2\sqrt{I_{B1}} = \sqrt{I_{out} + \frac{I_{in}}{1+m}} + \sqrt{I_{out} - \frac{I_{in}}{1+m}} \tag{8}$$

Squaring both sides gives the output current as

$$I_{out} = \frac{I_{in}^2}{4I_{B1}(1+m)^2} + I_{B1} \tag{9}$$

Eq. (9) describes the operation of the proposed squarer circuit. It is noteworthy that the output current is insensitive to PVT variations thanks to the benefits of using TL based structure. Another point is that 'm' sets the amount of current injected into the TL. Therefore, with a larger m, the input range can be extended significantly. The implementation of 'm' is realized through a set of switches that can be controlled by a digital code, as it is shown in Fig. 2 and is discussed in more details in Sections 2.2 and 3.1.

2.2. Current-mode multiplier circuit

The proposed current mode multiplier is shown in Fig. 3. It consists of two current mode squarers as discussed in Section 2.1 and a current subtractor. Each current squarer comprises a class AB current buffer and a TL. In order to implement m-transistors (M_{17}, M'_{17}, M_{16} and M'_{16}) two binary weighted transistors and a set of MOS switches are used. For instance, the M_{17} is implemented by transistors M_{20} (:1) and M_{21} (:2) and MOS switches of M_{s5}, M_{s6}, M_{s7} and M_{s8}. In a similar manner, M_{16} is implemented by transistors M_{18} (:1) and M_{19} (:2) and MOS switches of M_{s1}, M_{s2}, M_{s3} and M_{s4}. A 2-bit binary code (B_1B_0) controls these switches to provide four values of 'm' (0, 1, 2 or 3). It is shown in the following sections that selecting higher amounts of 'm' leads to improve the input range and linearity of the multiplier. The two TLs (M_1, M_2, M_3, M_4 and