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Dynamic Power Estimation using Transaction Level Modeling

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Abstract—**Designing an efficient (from performance and power points of view) system on chip (SoC) is one of the main challenges nowadays. This paper introduces a methodology that uses Transaction Level Modeling (TLM) to accelerate the simulation time for power estimation allowing fast SoC evaluation. Different modeling techniques are used to develop the proposed Transaction Level Power Modeling (TLPM) methodology. The methodology exploits abstracting the design using TLM. This abstraction allows fast simulation with still accurate functionality of the developed model. The methodology enables estimating power dissipation of real applications running on the SoC with high accuracy. ZYNQ-7000 platform is implemented on RTL and TLM to validate the methodology. The validation of the functionality is obtained through identical scenarios on both TLM and RTL. Experimental results reveal the efficiency and accuracy of the TLPM. The proposed methodology speeds up the simulation time by more than two orders of magnitude over RTL while the error in power estimation is less than 3%.**

Index Terms—**RTL, TLM, SoC, Power dissipation, Simulation time, SystemC**.

I. INTRODUCTION

SOCS are widely used nowadays in many applications such as mobile phones and digital cameras. Using Register Transfer Level (RTL) to model SoC has some limitations. The main limitation is the simulation time. As SoC complexity and size increase, the simulation of the full SoC on RTL becomes not practically possible. Accordingly, functional high level models should be used, but the accuracy of those models is very poor. High level models have little information about the underneath hardware details. Power profiling for a running operating system and real applications on the SoC requires innovative techniques. Modeling power dissipation of SoCs using TLM has a great impact on reducing the design life cycle [1], [2]. Accurate high level estimation saves the cost of the long iterations which elongate the design life cycle.

Previous approaches for power dissipation estimation at various abstraction levels of the design did not achieve satisfying accuracy [3–5]. Estimating power at high level of system abstraction has been addressed in [6]. Some important design elements such as power management components are missed in the previous approaches affecting the accuracy of the resulting power numbers versus actual on-chip ones.

Power Kernel tool flow [7–10] adopts cycle-accurate models in TLM. This leads to very large simulation time [11]. Power parameters characterization is done using extracted Gate level parasitics as in [6] and [8]. Power equations are constructed using the developed database of parasitics. The process of parasitic extraction and gate level simulation is time consuming and expensive. The simulation overhead is very large [12], [13]. Power dissipation is minimized at architecture level using Wattch framework. The accuracy is around 10% as compared to some verified tools [14]. Energy of the whole system at architecture level is calculated using SimplePower framework. It uses cycle-accurate data path which increases the simulation time [15]. Some simulation tools such as SimpleScalar are developed to provide architecture modeling. They use execution-driven simulation which increases the model complexity and leads to large simulation time [16–19]. For large SoC designs previous techniques/approaches are not efficient. The previous approaches are suffering from inaccuracy and slowness.

In this paper, a new approach (Transaction Level Power Modeling TLPM) is introduced for dynamic power estimation as shown in Fig. 1. Approximately-timed modeling is used to achieve fast simulation with high accuracy. Estimating dynamic power dissipation on Transaction Level Modeling (TLM) is developed in the proposed methodology [20]. The overhead in simulation to determine power dissipation is minimized. The error in calculating power dissipation is also minimized. It is shown in the paper that dynamic power estimation could be achieved in two phases. The extraction of power parameters from the RTL of a design is used to build Correlation Matrix in the first phase. This phase is called power characterization. In implementation phase, the power of RTL is mapped to TLM registers/ports to build power models on TLM as shown in Fig. 1.

The paper is organized as follows. In Section II, power characterization for Transaction Level Modeling is presented. In Section III, implementation of Transaction Level Power Modeling (TLPM) is provided. Applying the methodology on