Organic Electronics 24 (2015) 170–175

Contents lists available at ScienceDirect

Organic Electronics

journal homepage: www.elsevier.com/locate/orgel

Addressable growth of oriented organic semiconductor ultra-thin films on hydrophobic surface by direct dip-coating

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ARTICLE INFO

Article history:
Received 9 April 2015
Received in revised form 13 May 2015
Accepted 28 May 2015
Available online 29 May 2015

Keywords:
Patterning
Area-selective growth
Organic transistors
Dip-coating

ABSTRACT

Oriented organic field-effect transistor (OFET) stripe arrays on hydrophobic substrates were fabricated by fast dip-coating technique. The addressable growth was achieved by decreasing surface energy of the channel areas with respect to the electrodes via hydrophobic treatment. The higher surface energy of the electrodes allows solution to adhere and then organic semiconductors nucleate and bridge the channels after evaporation of the solvent. Area-selective behaviour can be controlled by adjusting surface property of transistor channel, geometry features of the gold electrodes, pulling speed and evaporation atmosphere. The mechanism behind is the competition between receding of the solution and evaporating of the solvent that generate the organic semiconductor films on the substrate. The patterned bottom-contact transistor arrays exhibit carrier mobility of 2.0×10^{-3} $cm^2 V^{-1} s^{-1}$, while no field-effect characteristics can be detected for bottom-contact arrays without hydrophobic treatment. Such reliable, fast and solution-based patterned OFET arrays are highly desirable for large-scale and low-cost production.

1. Introduction

Organic field-effect transistors (OFETs) have been regarded as the key basic components for many cutting-edge applications including sensors, displays, electronic papers, and radio frequency identification tags [1–3]. Solution-based process has been proven to be one of the important techniques, as they can save fabrication cost dramatically [4,5]. More inspiringly, the performance of OFETs can be comparable to that of the commercial polycrystalline silicon FETs. For instance, up-to-date reports show that the field-effect mobility for solution-processed small molecules and polymers OFETs can even be as high as 43 $cm^2 V^{-1} s^{-1}$ and 23.7 $cm^2 V^{-1} s^{-1}$, respectively [6,7]. However, to fabricate arrays of devices and integrated circuits, it is crucial to eliminate parasitic current paths (i.e., crosstalk) between neighbouring devices [8,9]. Patterning of OFETs is thus necessary but still remains a great challenge for large-scale fabrication, especially for solution processes.

To tackle this problem, researchers have developed two main strategies to grow thin films with predetermined patterns on the surface for solution-processed transistors. One is pre-designed templates for solution to permeate, and then organic molecules would nucleate in the channel arrays. Stamp printing [10], push coating [11], drag coating [12], self-organized [13] and solution shearing [14] are frequently used to control the flow or absorption of the solution. The other is pre-patterning separated wetting and dewetting regions. The solution would gather into wetting areas due to the repulsive force from the dewetting regions [9,15–21]. Much progress has been made during the recent years. However, there are still some important issues that are not easy to address. One is the dilemma between performance and patterning high quality films. For instance, the films grown on hydrophobic surface like self-assemble monolayer (SAM) modified surface usually gain better performance than hydrophilic surface like SiO_2. However, patterned growth of films on hydrophobic surface is not well assessable, owing to the dewetting or solvent repelling property on hydrophobic terminated group of SAM.

In this work, we report a simple method for selective growth of highly ordered molecular films in the hydrophobic regions with solution preparation. A simple dip-coating technique guarantees the fast and high throughput process. The addressable growth of the film ensures the formation of large area transistor arrays eliminating crosstalk. More importantly, this selective growth behaviour can be easily tuned by substrate modification and

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http://dx.doi.org/10.1016/j.orgel.2015.05.038
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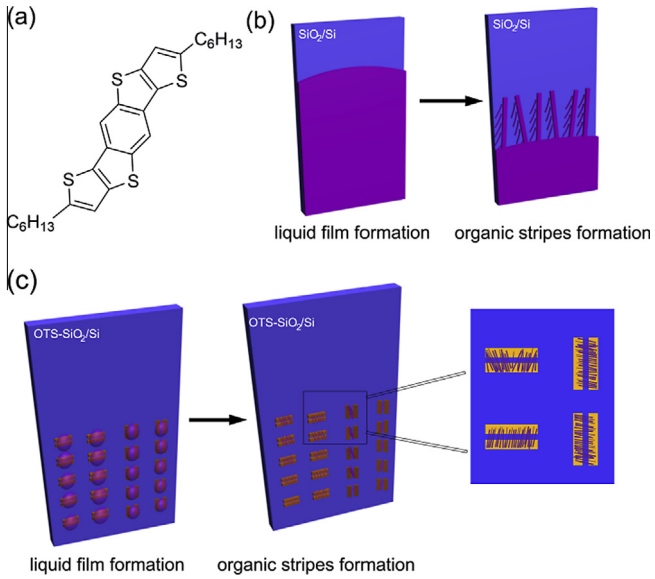

Fig. 1. (a) Molecular structure of DTBDT-C6. Schematic diagrams of the DTBDT-C6 stripes formation on substrates on (b) bare Si/SiO_2 and (c) OTS-treated and gold-patterned Si/SiO_2.

pre-patterning design. Spatial selectivity and large-scale uniformity of ultrathin films (<10 nm) were achieved and potential application on large-scale transistor arrays was demonstrated.

We use 2,7-dihexyl-dithieno [2,3-d;2′,3′-d′]benzo[1,2-b;4,5-b′] dithiophene (DTBDT-C6) (shown in Fig. 1a) as the organic semiconductor material, which tends to form micro-stripes on SiO_2/Si surface by dip-coating from toluene solution [22,23]. On pure hydrophobic substrate, it is impossible to form a film. By introducing hydrophilic patterned gold electrodes and changing the evaporation atmosphere, controllable area-selective growth of ultrathin stripes on hydrophobic substrate can be achieved.

2. Experimental section

2.1. Materials and thin film fabrication

DTBDT-C6 was synthesized according to the literature 28 and dissolved in toluene (Aldrich 99%, anhydrous) to form a 2 mg mL^{-1} solution. *P*-doped silicon with 300 nm SiO_2 (C_i = 10 nF cm^{-2}) was used as substrates. For octadecyltrichlorosilane (OTS) modified substrates, the Si/SiO_2 substrates were dipped into an OTS solution (hexane and chloroform, 7:3 in volume), the dip time was varied to generate surfaces with different hydrophobicity. Gold was thermally evaporated on the substrate through shadow mask to form patterned electrodes by using a Nano 36 thermal evaporator (Kurt J. Lesker Company, USA). Films of DTBDT-C6 were fabricated through vertical dip-coating with various pulling speed from toluene solution under ambient condition.

2.2. Film characterization

Atomic force microscopy (AFM) measurements were conducted with a Bruker Dimensional Icon in tapping mode, Silicon cantilever with a spring constant of 40 N m^{-1} was used. Scanning electron microscope was carried out using Zeiss Gemini Supra 55 (Oberkochen, Germany). XRD were performed in beamline of BL14 in Shanghai synchrotron radiation facility. The transistor performance was measured in air by a Keithley 4200SCS

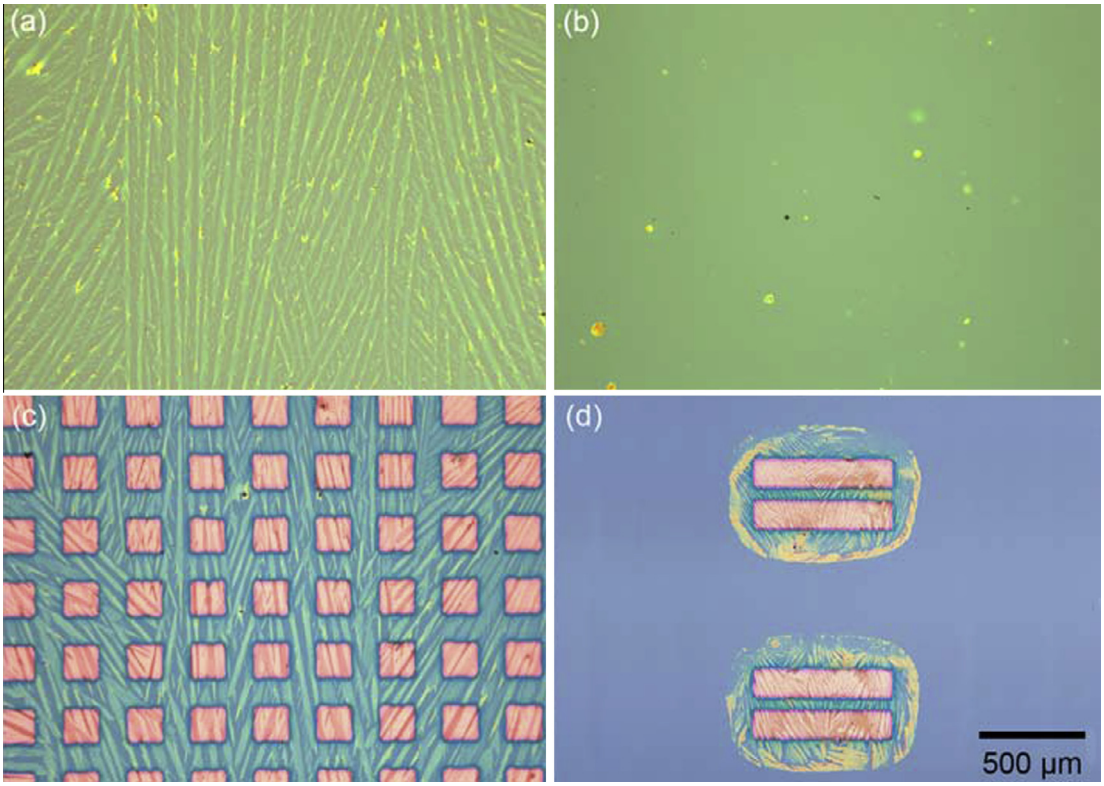

Fig. 2. Optical microscopy of DTBDT-C6 films on (a) bare Si/SiO_2 substrate, (b) OTS-treated Si/SiO_2 substrate, (c) OTS-treated Si/SiO_2 substrate with square patterned gold electrodes (100 μm * 100 μm pad with 100 μm channel) and (d) OTS-treated SiO_2/Si substrate with rectangle patterned gold electrodes (600 μm * 80 μm, channel: 50 μm). The pulling speed was 2000 μm/s.