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Reversibility of humidity effects in pentacene based organic thin-film transistor: Experimental data and electrical modeling

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ABSTRACT

P-type organic thin-film transistors (OTFTs), in which the active semiconductor is made of pentacene with silicon dioxide as a gate insulator, were fabricated and characterized. The effects of humidity on the electrical characteristics of pentacene based thin-film transistors (pentacene-TFTs) in the linear and saturation regimes were investigated. We report the variation of the electrical parameters by relative humidity (RH) extracted from the experimental electrical characteristics current–voltage of pentacene-TFT devices. We show that the diffusion of water molecules (H_2O), the creation of acceptor states due to the presence of oxygen and the formation of clusters in the pentacene active layer considerably affect the stability and the performances of pentacene-TFTs. The degradation of electrical parameters of the pentacene-TFTs under relative humidity (RH) can be recovered with a simple pumping under vacuum (3×10^{-5} to 5×10^{-5} mbar). We also show that the changes introduced by the effects of humidity are reversible. Moreover the pentacene-TFT presents an intensive response for a high relative humidity (RH = 57%), which could be used for a humidity detection device technology.

1. Introduction

Organic thin-film transistors (OTFTs) have received intensive interest because of their many advantages such as light-weight, low cost manufacture, structural flexibility and low temperature processing [1–3] that make them promising candidates in several areas of technology including gas sensors, smart cards, active-matrix displays and radio-frequency identification tags [4–8]. On the other hand, OTFTs provide multiple detection parameters like the inverse subthreshold swing (SS), the threshold voltage V_{th}, the field-effect mobility μ_{FET}, the current ratio I_{on}/I_{off} and the turn-on voltage V_{on} [9]. The stability of organic transistors represents a major challenge that must be addressed for making this technology relevant and reliable. Therefore, the influences of environmental effects on the electrical stability of the OTFTs have been extensively studied in recent years [10–13]. The electrical performances of unencapsulated organic devices (including thin film transistors) degrade when exposed to humidity [14–16]. The study of the influence of oxygen and water molecules on the characteristics of organic transistors is a crucial way for a best understanding of the interaction mechanisms between the organic active layer and these chemical species and their consequences on the performance of the device. Furthermore, the influences of impurities and structural properties of the organic semiconductor films have been widely investigated [17–19]. In addition, the progress and the improvement in the sensors technology based on OTFTs, such as sensors of temperature, pressure, gas, humidity and photo-detectors are directly related to the response and the sensitivity of the active layer of the transistor to external disturbances such as the temperature, illumination and humidity.

The main aim of this work is to report the effects of the humidity on the electrical stability of pentacene based TFTs in the linear and the saturation regimes. Accordingly, the electrical parameters characterizing the transistors were extracted from experimental data in different measurement conditions. In particular we have characterized the pentacene-TFTs under vacuum and under different relative humidity (RH) conditions. RH is defined as the ratio of the water vapor density (mass per unit volume) to the saturation water vapor density usually expressed in percent. Electrical characterization was done under vacuum (3×10^{-5} to 5×10^{-5} mbar), under different relative humidity (RH = 3% and RH = 57%), and finally under nitrogen (N_2) +RH = 3%. In the last experiment, the sample was subjected to a vacuum process for 48 h in order to study the reversibility of the degradation.

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Finally, we have developed an analytical model to reproduce the experimental output characteristics for two measurement conditions (under vacuum and under RH = 57%).

2. Experimental details

Fig. 1 shows the schematic structure of the fabricated pentacene-TFTs used in the present work. We have used a bottom-gate top-contact structure. A highly p-doped crystalline silicon wafer (p-Si) was used as a substrate. The Si substrate was cleaned sequentially by acetone, methanol, and de-ionized water in an ultrasonic bath for 10 min at each step. The SiO_2 layer of 300 nm was grown on the p-Si substrate in a furnace at 1000 °C for 2 h and it was used as the gate-insulator. Then, a pentacene ($C_{22}H_{14}$) layer (40 nm thick) was deposited on top of the SiO_2 by thermal evaporation in a high vacuum chamber (3×10^{-6} mbar). Finally, 80 nm gold (Au) source and drain electrodes were deposited by thermal evaporation under high vacuum (10^{-8} mbar) to obtain high quality ohmic contacts with the pentacene thin film. The deposition rates and the thicknesses of the pentacene and metallic layers were determined by a quartz balance. The channel length (L) and width (W) were 50 μm and 3760 μm, respectively, and they were defined using a shadow mask during the gold (Au) evaporation. The electrical characteristics and environmental stability of pentacene-TFTs were measured by using a manual Karl Süss probe and two programmable source-meters (Keithley 2400). The characterization under relative humidity (RH) was carried out by using a humidification system constituted of a water reservoir, three valves and two mass flow controllers enabling a gas flow regulation between 0 and 200 sccm. The measured relative humidity at the output of the system varies between 2% and 79%.

3. Results and discussion

3.1. Output characteristics of the pentacene based TFT under different measuring condition

Fig. 2(a)–(e) shows the output characteristic (I_D versus V_D) curves of the fabricated pentacene-TFTs. The drain voltage (V_D) was varied from 0 to −80 V in −1 V increments at different gate voltages (V_G) ranging from 0 to −40 V with −10 V increments. The measurements were carried out using five different conditions. Firstly, the measurement was made under vacuum (3×10^{-5} to 5×10^{-5} mbar) and repeated again after 30 min under RH = 3%.

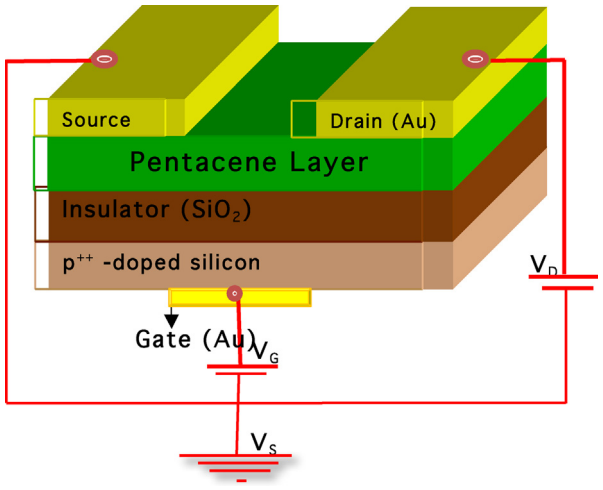

Fig. 1. Schematic diagram of a bottom-gate top-contact pentacene-TFT.

A third measurement was carried out after 30 min under a high RH level (RH = 57%), followed by a measurement after 30 min, in which the device was subjected to a flow of dry nitrogen in order to reduce the relative humidity toward RH = 3%. Finally, we have made the measurement under vacuum after two days of pumping.

The resulting output characteristics of the pentacene-TFTs (Fig. 2(a)–(e)) shows a typical p-channel operation. All the transistors showed a clear linear increase of the drain current at low drain voltages (linear regime), followed by a saturation at larger voltages (saturation regime) for all the experimental conditions. An exception was observed for the transistors subjected to a RH = 57% (Fig. 2(c)). For these transistors the saturation of the drain current was not observed. This behavior is attributed to the diffusion of H_2O molecules in the thin film of pentacene which increases the current I_{off} and prevents the saturation of the output characteristics [20]. Moreover, we note that the drain current increases by increasing the gate voltage in all the measurement conditions.

3.2. Transfer characteristics of the pentacene TFT in linear and saturation regime

3.2.1. In linear regime

In Fig. 3, we represent the transfer characteristics ($|I_D|$ versus V_G) for all the measurement conditions in the linear regime for a fixed drain voltage ($V_D = -10$ V) and by varying the gate voltage (V_G) of −50 to 50 V with 0.2 V increments. We note that there is a significant decrease in the absolute value of the drain current of pentacene TFT with the humidity for high negative gate voltages.

3.2.1.1. Series resistance of the pentacene TFT. The electrical performance of the OTFTs was mainly limited by the resistance effects. These effects are directly related to the increase of the charge carrier density in the channel of the transistor. Several methods have been developed for the extraction of the series resistance in OTFTs [21,22]. In the linear regime, the transconductance g_m can be defined as [23]:

$$g_m = \left[\frac{\delta I_D}{\delta V_G}\right]_{V_{D=cte}} = \frac{W}{L}\mu_{FET,lin} C_i V_D \quad (1)$$

where Wand L are the channel's width and length of the transistor, respectively, C_i is the insulator capacitance (per unit area), V_D is the drain voltage fixed to −10 V and $\mu_{FET,lin}$ is the field effect mobility in the linear regime that can be calculated through the following equation [24]:

$$\mu_{FET,lin} = \frac{L}{C_i V_D W}\left[\frac{\delta I_D}{\delta V_G}\right]_{V_{D=cte}} = \frac{L}{C_i V_D W} g_m \quad (2)$$

In this regime, the expression of the series resistance of the pentacene-TFT is defined as follows:

$$R_s = \frac{1}{g_d} - \frac{L}{W C_i \mu_{FET,lin}(V_G - V_{th})} \quad (3)$$

where g_d is the conductance $g_d = [\delta I_D/\delta V_D]_{V_{G=cte}}$, since in the linear regime we work at low drain voltage ($V_D = -10$ V) we can approximate the numerical derivative of the drain current on the drain voltage to the ratio of these quantities: $g_d = [\delta I_D/\delta V_D]_{V_{G=cte}} = I_D/V_D$ [23].

The other parameters were defined previously.

Fig. 4 shows the experimentally values of the series resistance R_s as a function of the gate voltage for the five measurement conditions. It is clear that the series resistance decreases rapidly for negative gate voltages because the increase in the density of charge introduced in the conducting channel. Furthermore, in the inset we have depicted the series resistance for positives gate voltages. It is