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Periodically patterned Si pyramids for realizing high efficient solar cells by wet etching process

Melvin David Kumar [a], Hyunyub Kim [b], Joondong Kim [a,*]

[a] *Department of Electrical Engineering, Incheon National University, Incheon 406772, Republic of Korea*
[b] *Research Division, Plansee Korea HPM Inc., Siheung 429926, Republic of Korea*

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Abstract

Periodic Si structures were designed for a high-efficient solar cell. Wet-etching method was applied to tailor the light-absorbing Si substrate to periodic patterns. Electrical conductor of a thin indium-tin-oxide (ITO) layer was coated onto the patterned Si structures as an anti-reflection coating layer, which effectively reduces the light-reflection at a surface. Due to the optical end electrical benefits of an ITO layer, the periodic Si solar cell provided much improved current density of 36.28 mA/cm^2 with a conversion efficiency of 16.3%. For quantum efficiencies, this ITO-coated periodic Si structure solar cell is enormously effective to improve long-wavelength photons. This study reveals that efficiency of solar cells could be readily enhanced via large-scale available wet-etching processes with an electrical conductive ITO coating method.

Keywords: Wet etching; Pyramid patterns; Si solar cells; ITO

1. Introduction

The solar cell research is a hot and higher progressive research field for past few decades because of increasing awareness to pursue the pollutant free energy (Karni, 2011; Trancik, 2014). An efficient photovoltaic device is expected to utilize as much incident photons as possible in order to attain high efficiency. Therefore, many research groups are carrying on their experiments in diversified platforms like Si based solar cells, dye sensitized solar cells, thin films solar cells, quantum dot solar cells, etc., to enhance the efficiency (Fonash, 2010; Yaacobi-Gross et al., 2011; Yum et al., 2014). The main objective of these experiments is to emerge with a photoelectric device which generates more number of free electrons by absorbing maximum number of incident photons. In the present article, the innovative and cost-effective research method to improve the optical and electrical performances of Si-based solar cells has been discussed. Inherently, Si has the low band gap energy of 1.1 eV which leads to limited light absorption (Hu and Chen, 2007). However, the patterned Si substrates with different structures increase the proficiency of the devices due to their low reflection and reduced resistivity (Diaz-Quijada et al., 2011; Huang et al., 2009; Lee et al., 2013; Mukherjee et al., 2009; Zeballos et al., 2010). Surface enlargement via patterning of Si substrates provides the initiative solution to acquire the enhanced optical and electrical properties. Recently, few advanced methods such as ion beam lithography, electron beam lithography and focused ion beam milling have been used to structure the Si substrates in micro and nano

* Corresponding author.
E-mail address: joonkim@incheon.ac.kr (J. Kim).

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dimensions. Nevertheless, these methods produced better results only in the small scale fabrications and few results were found yet with the efficiencies more than 15% when large areas to be structured (Jeong et al., 2013; Krogstrup et al., 2013; Kulakci et al., 2013). In addition, they are cost wise expensive. The pattern formations on Si substrates using chemically etched masks are the most viable and the best alternative to the above said processes. The most commonly used etching processes are wet etching, reactive iron etching, dry etching and plasma etching. Among them, wet chemical etching process is the facile and cast effective method to prepare patterned Si substrates which are used for potential applications (Peng et al., 2002, 2004). These beneficial structures could be further improved by covering them with thin layer of anti-reflection coating. Especially, ITO layer is well suited to be coated over the patterned Si structures due to its unique properties of high transparency, low resistivity, high carrier concentration, wide energy band gap and eminent work functions (Schlaf et al., 2001; Yun et al., 2013; Zhang et al., 2012). Moreover, the ITO layer can perform various roles such as ohmic contacts, rectifying junctions, anti-reflectors and passivation layer proficiently.

In the present work, we have demonstrated the efficiency of 16.3% for wet etched Si pyramid structure. This is relatively higher efficiency when compared to 13.7% of all back contact Si solar cells (Jeong et al., 2013). The defect free surface, desired patterns to enlarge the surficial length, adjustable depth to avail maximum light absorption and short carrier collection length are the important features of adopting wet etching method in photovoltaic industries. The characteristics of wet etched Si pyramid structure were compared to those of flat reference Si substrate in the motive to explore the effectiveness of structured Si substrates and wet chemical etching method. In the present scenario of photoelectric research, this report would be more useful for the researchers to fabricate the desired patterns on Si substrates via cost effective methods and to achieve the improved efficiency.

2. Experimental procedure

The Si pyramid structure was patterned on a 4 in. Chokralsky (CZ) grown 500 μm thick, p-type (1 0 0) Si wafer having a resistivity of 1–10 Ω cm via chemical wet etching. As a first step of this process, the Si substrates were masked with photoresist (PR) pattern which was prepared by spin coating method at 3000 rpm for 30 s to have 2 μm thicknesses. After exposing UV light at 200 W, the PR patterns were developed. Then SiO_2 layer was deposited on the pre-coated PR pattern to make SiO_2 pillar arrays by sputtering method. A lift-off procedure was followed to remove the template of PR pattern, leaving SiO_2 pillar arrays on a Si substrate. A detailed schematic representation of preparation method is shown in Fig. 1. The base substrate with SiO_2 mask was undergone wet etching process for 10 min. The wet-etching solution was prepared by mixing of NaOH (2.5 wt%) and isopropyl alcohol (5 wt%) in the base of de-ionized water (92.5 wt%). The prepared solution was maintained at 60 °C during the fabrication process. During the wet etching process, the areas covered by SiO_2 mask were protected from being etched out, resulting in the formation of periodically patterned Si pyramids. The SiO_2 mask was easily removed by hydrofluoric solution after the etching process. Each Si pyramid has a height of about 2.08 μm with a width of about 3.5 μm. Then, p–n junction was formed by flowing phosphorous oxychloride ($POCl_3$) as an n-type doping agent, in a furnace at 800 °C temperature for 40 min. After the junction formation, a buffered hydrofluoric acid (5% HF) solution was used to remove phosphor silicate glass (PSG). At this stage, a thin ITO layer of 80 nm thickness was deposited by supplying the DC power of 300 W to a 4-in. ITO target (In_2O_2 containing 10 wt% SnO_2) at room temperature (RT) under Ar atmospheric condition using DC sputtering system (SNTEK, Korea). The top ITO film passivates the n-type doped emitter Si layer and also works as an anti-reflection coating. The prepared samples were tailored to a size of $3.2 \times 3.2\ cm^2$. For the electrodes purpose, the Ag paste (Ferro 33-462) and Al paste (Ferro 53-102) were screen printed on front and back side of the devices respectively. Then, the electrodes were undergone the co-firing process in a belt furnace at a temperature of 850 °C.

The surface morphology of pyramid structured Si device was observed by field emission scanning electron microscope (FESEM, FEI Sirion). The optical properties of the prepared samples were characterized using UV spectrophotometer (Scinco, Neosys-2000). *I–V* characteristics were analyzed using a simulator system (McScience-K3000) under one-sun ($100\ mW/cm^2$) illumination by using a power meter (McScience-K101). Quantum efficiency measuring system (McScience-K3100) was employed to measure internal and external quantum efficiencies.

3. Results and discussions

3.1. Structural properties

During the etching process, the time-to-time formations of Si pyramid structure on the substrate were recorded using FESEM as shown in Fig. 2(a–l). From Fig. 1, it is well seen that the performance of wet-etching process is perfect in structuring the Si substrates. The uniform array of Si patterns with identical spacing was observed from the titled images of the samples. The prepared wet etching solution is sensitive to etch the portions which are not covered with SiO_2 deposition. Therefore, it has created a depth of 318 nm around SiO_2 coated regions within a minute of etching time as shown in Fig. 2(a) and (g). When etching time is increased, the depth also is increased and Si pillar structures are gradually transformed into accurate pyramids over a time of 10 min. The pyramid structure which was formed as a result of 10 min wet etching is used for further characterizations. The etching depth with respect to the etching time showed almost linear behavior which is determined from Fig. 3. There were no sudden changes in