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Device optimization and scaling properties of a gate-on-germanium source tunnel field-effect transistor

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ABSTRACT

A gate-on-germanium source (GoGeS) tunnel field-effect transistor (TFET) shows great promise for low-power (sub-0.5 V) applications. A detailed investigation, with the help of a numerical device simulator, on the effects of variation in different structural parameters of a GoGeS TFET on its electrical performance is reported in this paper. Structural parameters such as κ-value of the gate dielectric, length and κ-value of the spacer, and doping concentrations of both the substrate and source are considered. A low-κ symmetric spacer and a high-κ gate dielectric are found to yield better device performance. The substrate doping influences only the p–i–n leakage floor. The source doping is found to significantly affect performance parameters such as OFF-state current, ON-state current and subthreshold swing, in addition to a threshold voltage shift. Results of the investigation on the gate length scaling of such devices are also reported in this paper.

1. Introduction

Owing to different current injection mechanism, a tunnel field-effect transistor (TFET) can overcome the subthreshold swing (SS) limitation of a conventional metal–oxide-semiconductor FET (MOSFET) [1–5]. The main challenge to a TFET has, however, been to improve its low ON-state current

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I_{ON}. Recently, both experimental and simulation results demonstrate [2,6–12], that a TFET, in which vertical carrier tunneling (i.e., carrier tunneling in line with the gate electric-field) is dominant, can meet the I_{ON} requirement for sub-0.5 V operation, due to the larger area of tunneling in such devices.

Compound semiconductor-based vertical tunneling FETs have, however, a few major challenges, such as: (i) a large SS and, hence, a large OFF-state current I_{OFF} and (ii) a large ambipolar current [6,7], in addition to the processing issue. Higher dielectric constant results in a larger semiconductor capacitance that, in turn, gives rise to a large SS in such compound semiconductor-based devices than the silicon devices. I_{OFF} and SS for an L-shaped Ge source device, as proposed in [8], are also substantially high in the absence of a technologically challenging SiO_2 isolation layer between the source and drain under the channel. Although the silicon vertical tunneling FET structure that uses an ultrathin epitaxial channel region [9–11] or the Ge electron–hole bilayer TFET [12] appear promising, no experimental demonstration of these structures is available yet. The relatively low SS and I_{ON} for the Ge-source TFET in [2] are due to the occurrence of lateral carrier tunneling [13]. To improve SS and I_{ON}, an elevated Ge-source TFET is proposed in [13]. Improvement is achieved in such a structure by suppressing the lateral carrier tunneling. The stringent requirements of uniformity and quality of the ultrathin spacer layer in such elevated TFETs make the fabrication of such devices technologically challenging. Moreover, the gate capacitance for such a device in [13] as well as for the U-shape channel device with a SiGe source, as proposed in [14], is very large owing to the large effective channel length that would degrade switching characteristics. A novel device structure for a gate-on-germanium source (GoGeS) TFET is proposed recently in [15] that not only eliminates the above difficulties of an elevated Ge-source TFET but also achieve both supersteep SS and high I_{ON} enabling sub-0.5 V operation. In this paper, an investigation of the effects of different structural parameters, such as κ-value of the gate dielectric, length and κ-value of the spacer, and doping concentration of both the silicon substrate and germanium source, on the performance of a GoGeS TFET is reported. The effects of gate length scaling are also investigated.

2. Device structure and simulation setup

A cross sectional view of the *n*-channel GoGeS TFET, used in this study, is shown in Fig. 1. The highly doped *p*-type Ge region, the moderately doped *p*-type Si substrate, and the highly doped *n*-type Si region act as the source, channel, and drain, respectively. The device may be implemented on a bulk Si substrate following the process steps shown in Fig. 2 [15]. After shallow-trench isolation, a dummy gate consisting of SiO_2 and polysilicon may be defined over the intended drain region, which is followed by the formation of the first spacer and the first silicon recessing Fig. 2(a) to form a step in the silicon channel region. The first silicon recessing may be carried out by either anisotropic dry etching or oxidation followed by wet etching. Both the lateral diffusion during drain implantation (to be performed later) and undercutting of the silicon during first silicon recessing should be considered in determining the width of the first spacer layer. The second spacer may be defined next, which is

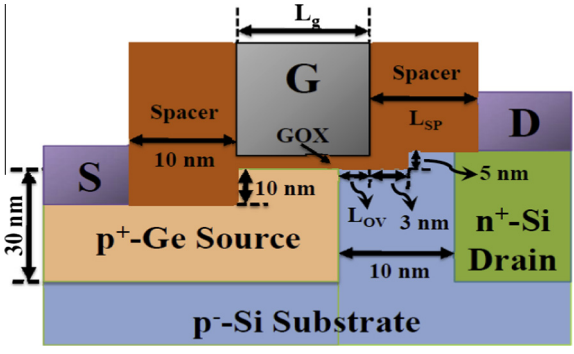

Fig. 1. Device structure of the *n*-channel GoGeS TFET.