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Reduction of harmonics in grid-connected inverters using variable switching frequency

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ABSTRACT

The increasing application of distributed power generation into the power system makes grid interconnection requirements of power quality more and more stringent. The reduction of current total harmonic distortion (THD) of grid-connected inverters to achieve the grid code by increasing of switching frequency in PWM of inverters is one of the popular methods, but this increases the switching loss. The aim of this paper is to propose a PWM technique with the function of variable switching cycle to reduce the current harmonics in grid-connected inverters. The weights of this function are determined by using a genetic algorithm under the constraint of constant switching loss. The simulation and experimental results of the proposed technique as well as the conventional constant technique are given and compared, which validate the performance of the proposed technique.

Introduction

There is increasing application of distributed generations into power system such as wind, solar energy, and fuel cells owing to the strong development of grid-connected inverter systems [1] for sustainability and the environment with enormous potentials [2]. However, grid-connected inverters significantly generate current harmonics into power network and adversely affect the power quality of the system. So, the harmonic attenuation is expected to be significantly more stringent to meet IEEE standard 929-2000 [3], 1547-2009 [4,5]. The inverters of sine pulse-width modulation (SPWM) are very popularly used in renewable energy converters [6–9]. To reduce the output current harmonics of these grid-connected inverters, the increase of inductance in filters is one of the popular methods, but it also has the disadvantages of costs and sizes of devices. The increase in switching frequency to reduce the current harmonics of inverters is also a different method, but higher switching frequency results in higher switching loss and overheating in components [10].

The technique in [11] used the H∞ controller instead of the conventional PI controller in conditions of grid impedance variations with enough high-frequency attenuation to keep the control loop stable. However, this technique also requires time and knowing the parameters of the grid to track the weighting functions. Therefore, the determination of weighting function is complex and the calculation a burden.

An SPWM-based variable switching frequency technique in [12] proposed to reduce the switching loss of inverters also requires the accurate model of ripple current and the complicated calculations cause robustness and low dynamic response. In addition, the use of very high range of switching frequency is not suitable for semiconductor switches of real grid-connected inverters. Moreover, the high ripple caused by very low switching frequency at the vicinity of zero of current is a big obstacle to digital electronic devices and electric motors.

A different technique with variable switching frequency in [13] was based on the estimated model of total demand distortion (TDD). However, the requirements of many parameters such as inductance of filter, dc voltage, ac voltage, current reference, time of computation to select the better switching cycle, and step variations of switching cycle according to load make the strategy perform with poor dynamic response and robustness. The uncalculated switching loss and the selected switching cycle only based on the limit of TDD in [4] are not optimal result for both current THD and switching loss.

The multilevel inverters in [14–18] are also used to reduce the current harmonic content, but they also have complicated control and many power switches increase the cost. To reduce the switching loss and current THD, the hysteresis technique in [19] exposed the dependence of measured current error and current sensor. Thus, it is also not robust.

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Recently, there are many heuristic methods [20] proposed for selective harmonic elimination in PWM inverter instead of solving equations of nonlinear transcendence such as genetic algorithm (GA) [21], particle swarm optimization (PSO) [22–24], ant colony optimization (ACO) [25], artificial bee colony algorithm [26], and artificial neural network [27]. However, the switching loss has not been considered in these methods.

This paper proposes a PWM technique with a variable switching cycle to reduce the current harmonics in grid-connected inverters. The optimal switching cycle of the inverter in every half of the fundamental period is determined by using genetic algorithm (GA) to reduce the current harmonics under the constraint of constant switching loss.

Currently, grid-connected photovoltaic (PV) systems come in many sizes and power capacities. Depending on the PV power plant configuration, the PV inverters can be categorized as module, string, multistring, and central inverters [28]. Most three-phase PV inverters are not true three-phase, three-wire inverters; rather, they are three-phase, four-wire inverters. Such inverters operate as three independent single-phase inverters. This solution enables the use of existing single-phase inverters and the 'mild' anti-islanding requirement from the German standard VDE-0126-1-1 (2006). In addition, the real problem of using a true three-phase, three-wire inverter is that the DC voltage needs to be relatively high (600–1000 V). In contrast, most inverters widely used in single-phase systems in residential applications are of the module and string types [29–31] and require a lower DC voltage (approximately 400 VDC). PV systems remain dominant in residential applications and will exhibit even greater diversity in the future mixed grid. Therefore, in this paper, the current development of single-phase inveters should be selectively considered.

Approach method

Both the current THD and switching loss of the inverter depend on the switching frequency. In the conventional PWM technique with constant switching frequency, the higher switching frequency results in higher switching loss and lower current THD, and vice versa. Therefore, the selection of optimal switching frequency to reduce the current THD of inverters is a complicated problem and has a very important meaning in power quality.

An H-bridge grid-connected single-phase inverter with unipolar PWM as shown in Fig. 1(a) is used for analysis in this paper.

It is assumed that the switching frequency of the inverter is much higher than the frequency of the control signal, effect of dead time is negligible, and the inductance of the filter is fixed.

The losses of IGBTs and diodes consist of conduction loss, switching loss, and other losses. It is also assumed that the conduction loss is not dependent on the switching frequency of the inverter and the switching loss linearly depends on the switched fundamental current and switching frequency in one switching cycle.

Based on the superposition principle, the inverter output current consists of the fundamental current and the ripple current.

The waveforms in Fig. 1(b) shows that the output current of the inverter increases and decreases in every half of the switching cycle of the carrier wave. In the positive half cycle of the carrier cycle, the increase of peak-to-peak current ripple i_{L1} can be calculated as

$$i_{L1} = \frac{[1 - d(t)]}{L_f} d(t) \frac{T_s}{2} V_{dc} \tag{1}$$

where L_f is the inductance of the output filter of the inverter, V_{dc} is the DC input voltage value of the inverter, $d(t)$ is the duty cycle, and T_s is the cycle of the carrier wave.

A similar calculation for the decrease of current ripple i_{L2} is as follows:

$$i_{L2} = \frac{|1 + d(t)|}{L_f} [-d(t)] \frac{T_s}{2} V_{dc} \tag{2}$$

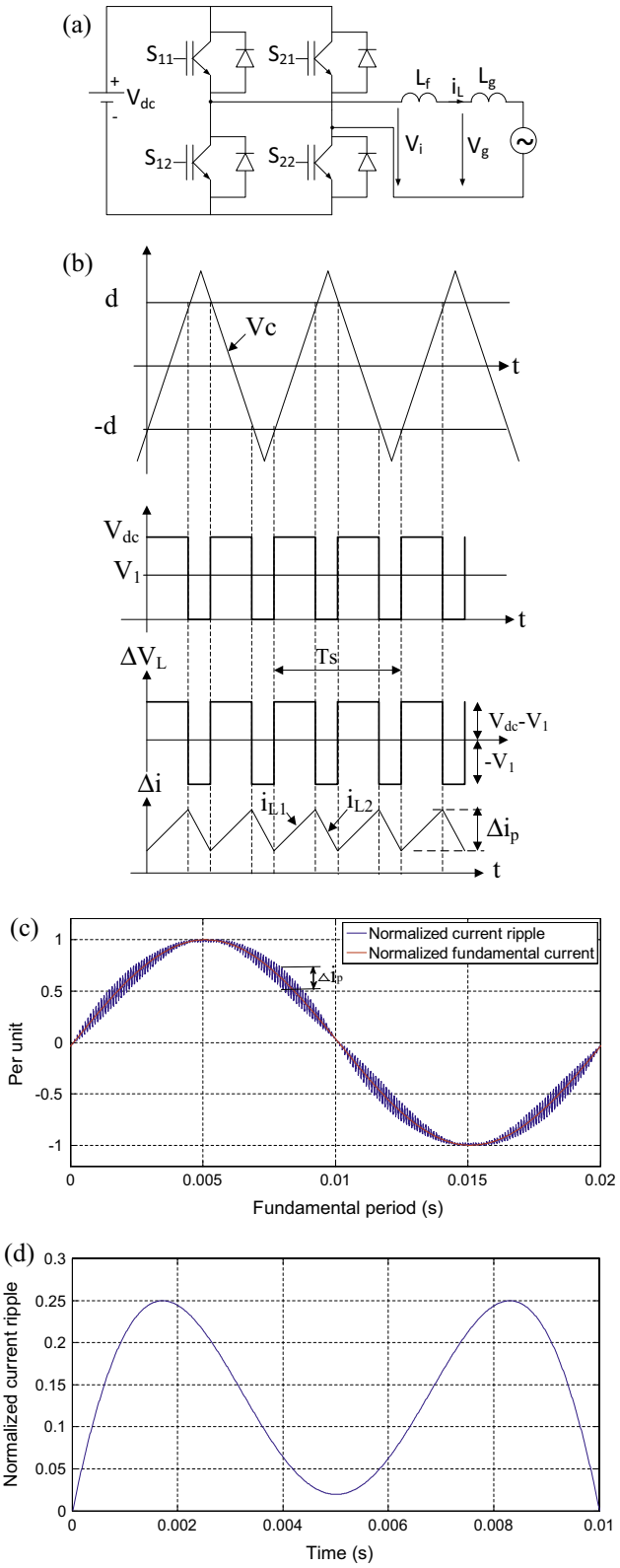

Fig. 1. Single-phase inverter with unipolar PWM. (a) H-bridge grid-connected inverter. (b) Carrier wave, voltage ripple, current ripple. (c) Output current waveform of unipolar H-bridge single-phase inverter. (d) The current ripple distribution in half of fundamental period ($m = 0.97$).