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Brief Papers

# An efficient hardware implementation of a novel unary Spiking Neural Network multiplier with variable dendritic delays ☆

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ABSTRACT

We propose a novel unary spiking circuit for a serial multiplier with variable dendritic delays. Serial multipliers commonly use the soma model for the arithmetic operation. The structure of the serial multiplier and the efficient implementation of the dendritic delays on customized neuromorphic hardware are the major contributions of this work. The design of the multiplier was inspired by the biological processes of dendrites, which use feedback connections and dendritic growth to synchronize the neural processing performed by the soma. The multiplier eliminates complex rules by adopting the soma model with dendritic connectivity configurations, increasing the processing speed compared with previously reported solutions based on Spiking Neural Networks.



## 1. Introduction

Spiking neural multiplication circuits are modeled on biological neural processing. Their main objective is to increase the capabilities of existing conventional circuits, enabling them to process larger amounts of information and very large numbers, adding possible applications of the devices, e.g., image filtering or cryptography. These classes of spiking neural circuits have made possible the development of a new branch of science, *Biologically Inspired Engineering*.

Several neural multiplier circuits employing Spiking Neural P (SN P) systems have been developed to create compact systems with higher processing capabilities, whose foundations are conceptualized as distributed parallel computing devices [1]. The SN P circuit model is based on the behavior of the soma and the circuit process information using a unary codification of events (spikes), which mimics the brain's information coding, i.e., the number three is represented by a sequence of three spikes. Soma modeling employs two main kinds of rules: firing and inhibition. Based on these rules and the sequence of input spikes, the neuron can fire or forget the spikes. In a recent work [2] the authors posited a time-free SN P multiplier, where the neuron is free to apply or not its rules that are enabled by the number of spikes contained on it. In the cited approach, the time-free SN P multiplier uses 11 neurons, and it works under a unary codification.

The current trends in the development of neuromorphic hardware emphasize the need for enhanced processing speed to create efficient spiking neural emulators, while also supporting higher complexity neural dynamics. To achieve such purpose, the spiking emulators should exhibit the fundamental properties of neurons: high dendritic connectivity, dendritic delay and parallel processing. A limited number of works address at least two of these three aspects: high connectivity and dendritic delay. One of the most interesting of these proposals is given in [3], where a four-bit delay register is proposed to imitate the dendritic delay. In this work, the counter is contained in the register and it is set whenever the spike arrives. This strategy encloses the system capacity to process a spikes sequence for the processing of a single spike by virtue of enabling the counter whereas the remaining spikes are ignored.

This paper proposes a new approach to SN P systems, incorporating functional dendritic elements and employing the experimentally proven features exhibited by the biological dendrites, such as dendritic feedback and delay [4] and dendritic growth [5], to implement a simplified neuronal circuit.

The new circuit performs a multiplication, using a reduced number of neurons with simple rules, has a minimum hardware requirement and provides an improvement the processing speed.

## 2. Multiplier circuit

The formal definition of the SN P system was posed in [1]. Where the spikes are treated by means of spiking rules of the form

☆Fully documented templates are available in the elsarticle package on CTAN.

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$E/a^c \to a^p : d$, here $E$ is a regular expression over a symbol, $a$ and $c$, $d$, $p$ are natural numbers, $c \geq 1, d \geq 0, p \geq 1$. This rule means that if a neuron containing $k$ spikes where $a^k \in L(E), k \geq c$, then it consumes $c$ spikes and produce $p$ spikes as an output, after a delay $d$ of steps. Then the spikes are sent to the connected neurons through the synapses. Also, there are *forgetting rules*, of the form $a^s \to \lambda$, which implies that $s \geq 1$ spikes are removed, provided that the neuron contains exactly $s$ spikes. Our model possesses novel characteristics related to dendritic delays in SN P systems. We contend that these dendritic delays are of special relevance, despite the opposing view of several computational neuroscientists who discarding them as a nuisance, that only complicates the model as it was described in [6]. Furthermore, Izhikevich demonstrates that a spiking network system with delays improves the information processing function and that this improvement is a consequence of the stable firing patterns, remarking that it is not clear how to obtain equivalent results when delays are discarded. More precisely, the dendritic delays work as a synchronizer providing stable incoming firing patterns.

To include the dendritic model in the formal definition of SN P systems [1], three generalizations of this model have been developed. The first generalization is based on the inclusion of delays. The second one is mainly focused on dynamic dendritic growth (both delays and dynamic growth are observed in biological dendrite behavior). The third generalization includes dendritic feedback. We shall explain these concepts further, along with the introduction of the SN P multiplier.

The proposed SN P multiplier system $\prod_{mul}$ uses a unary codification by firing a sequence of spikes whose output is determined by the simple product of two positive integers, $x \times y$. The circuit employs three neurons to calculate the product of two positive integers $x$ and $y$. The neurons $\sigma_{in_1}$ and $\sigma_{in_2}$ are proposed to act as input units, while the neuron $\sigma_F$ the system output, as illustrated in Fig. 1. These three neurons are connected by four synapses, $syn_1$, $syn_2$, $syn_3$ and $syn_4$, where three of them incorporate particular dendritic behavior. The first $syn_1(\sigma_{in_1}, \sigma_F)$ denotes the *dendritic growth* [5], where the dendritic arborization grows due to the influence of the environment, dynamically improving the neural processing. A direct consequence of dendritic growth is a *dendritic delay* [4], represented as $\Delta t_{max1}$. $\Delta t_{max1}$ is enabled after detecting the first spike to mimic dendritic growth. Therefore, the first spike arrives immediately at the input of neuron $\sigma_F$, and the subsequent spikes are delayed by the action of the dendritic growth. The dendritic delay of $syn_4(\sigma_F, \sigma_{in_2})$, denoted $\Delta t_{max2}$, is constant and is enabled at every moment of the defined time. Finally, $syn_3(\sigma_F, \sigma_F)$ shows a *dendritic feedback* that can be viewed as a propagation medium for spikes traveling back to different kinds of biological neurons [4].

The proposed multiplier is implemented with dendritic delays $\Delta t_{max1}$ and $\Delta t_{max2}$ as follows:

$$\prod_{mul} = (O, \sigma_{in_1}, \sigma_{in_2}, \sigma_F, syn, \Delta t_{max1}, \Delta t_{max2}, in, out), where,$$

- $O = \{a\}$;
- $\sigma_{in_1} = (0, R_{in_1})$ with $R_{in_1} = \{a \to a\}$;
- $\sigma_{in_2} = (0, R_{in_2})$ with $R_{in_2} = \{a \to a\}$;
- $\sigma_F = (0, R_{F_1}, R_{F_2})$ with $R_{F_1} = \{a^2 \to a\}$, $R_{F_2} = \{a \to \lambda\}$;
- $syn = \{syn_1(\sigma_{in_1}, \sigma_F), syn_2(\sigma_{in_2}, \sigma_F), syn_3(\sigma_F, \sigma_F), syn_4(\sigma_F, \sigma_{in_2})\}$
- $\Delta t_{max1} = \{[(in_1, F) \to n+1]\}$
- $\Delta t_{max2} = \{[(F, in_2) \to n]\}$

The circuit $\prod_{mul}$ (see Fig. 1) multiplies two positive decimal integers with unary codification $x \times y$ as follows.

In the initial state, all neurons are without information, and there is no $\Delta t_{max1}$ in $syn_1(\sigma_{in_1}, \sigma_F)$. The input neurons $\sigma_{in_1}$ and $\sigma_{in_2}$ receive a sequence of spikes from the Spike Coder. Both neurons fire to neuron $\sigma_F$, which receives the spikes without any dendritic delay.

According its firing rules, neuron $\sigma_F$ fires a spike after receiving two spikes. The fired spike is sent to three destinations. The first is the final *output* of the system, which contains the arithmetic result of the multiplications. The second destination is $\sigma_F$ itself, because $\sigma_F$ has a feedback loop ($syn_3$). The third and last is the neuron $\sigma_{in_2}$. This last neuron imposes a dendritic delay of $\Delta t_{max2}$, which results in the delay of the incoming spikes of duration $n$. Notice that the number $n$ depends upon the magnitude of the input $y$.

Therefore, in the next step the neurons $\sigma_F$, $\sigma_{in_1}$ and $\sigma_{in_2}$ fire simultaneously and the delay $\Delta t_{max1}$ corresponding to the dendritic connection is set to $n+1$ steps (see Fig. 1) due to the

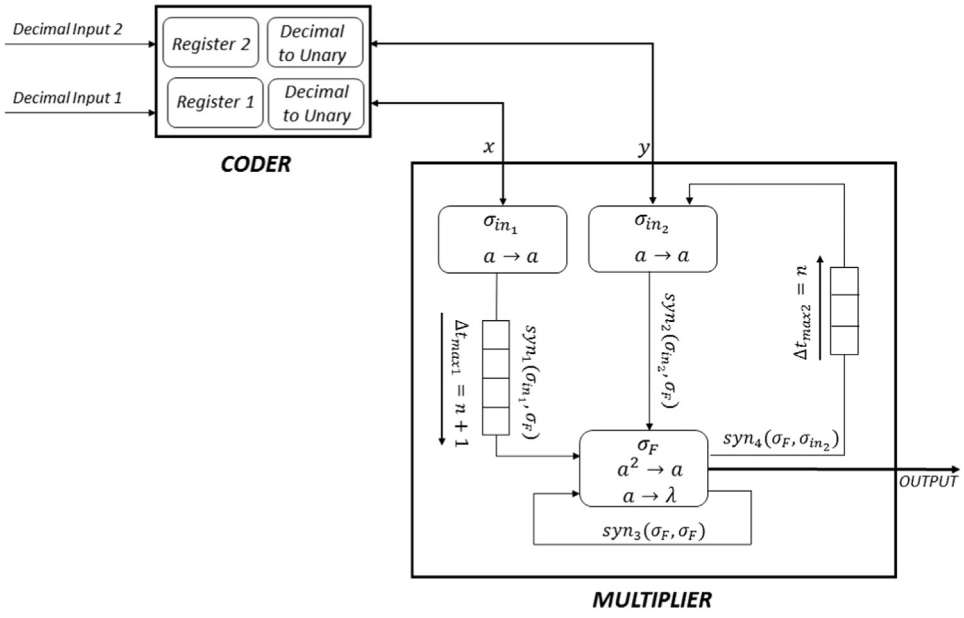


**Fig. 1.** Multiplication circuit exploiting dendritic feedback and dendritic delays.