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Transconductance and slew rate improvement technique for current recycling folded cascode amplifier

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ABSTRACT

A proposed technique to achieve transconductance and slew rate improvement of current recycling folded cascode amplifier is presented in this paper. It adopts the local common-mode feedback structure to increase gain-bandwidth, dc gain and slew rate of conventional recycling current amplifiers with no additional power dissipation. A proposed amplifier based on this technique is simulated on UMC 180 nm process. The simulation results demonstrate that the proposed amplifier achieves a 200% gain-bandwidth, 10 dB dc gain and 100% slew rate improvement with the same power dissipation when compared to the conventional current recycling counterparts.

1. Introduction

In switched-capacitor (SC) circuits, the operational transconductance amplifiers (OTAs) are critical analog blocks, which require fast settling response and precise final value [1]. Therefore, the high performance OTAs should have high dc gain, wide gain-bandwidth (GBW) and large slew rate [2]. In recent years, the current recycling folded cascode OTAs (RFC) get preferred over conventional folded cascode OTAs (FC), owing to the improved GBW, dc gain and slew rate [3,4]. Some techniques to further improve the effective transconductance and slew rate of RFC are also presented, such as current-shunt technique, positive-feedback technique and double-recycling technique [5–7]. In [5], current-shunt technique is employed in the cross-coupled current mirrors to separate dc and ac path of recycling structure, leading to a significant boost in GBW and slew rate. In [6], positive-feedback technique is utilized to form the positive-feedback current mirror loads to improve the gain of recycling structure, achieving the enhancement of general performance compared to RFC. And in [7], an increased recycling path is used to double recycling the input signal, improving the GBW and slew rate of RFC with no additional power. Although the presented techniques have improved the GBW and slew rate of RFC, all of them lower the location of first non-dominant poles, and thus degrade the phase margin, causing stability issues of OTAs.

In this paper, a proposed technique to achieve the enhancement of general performance, including the GBW, slew rate and dc gain, of the conventional RFC is presented. It is based on the local common-mode feedback structure, not only improving the effective transconductance and dc gain, but also boosting the slew rate [8–10]. Most of all, the enhanced performances introduced by this proposed technique are at no cost of power penalty and preserving stability.

This paper is organized as follows. The conventional RFC is discussed in Section 2. In Section 3, the amplifier based on the proposed technique to improve the transconductance and slew rate is described and the circuit performances including GBW, dc gain, slew rate, stability and noise performance are discussed. To demonstrate the enhanced performances of proposed technique, two OTAs are designed and compared in Section 4. And the conclusions are given in Section 5.

2. The conventional RFC amplifier

The conventional RFC is shown in Fig. 1 [3,4] where all transistors operate in the saturation region. The input differential pairs is split to $M1a$ and $M1b$. Transistor $M1b$ is used to recycle input signal current, which is then amplified by a factor of K through cross-over mirror current $M3$:$M2$. Thus, the equivalent transconductance (G_m) of RFC is given as [3,4],

$$G_{mRFC} = (K+1)g_{m1a} \quad (1)$$

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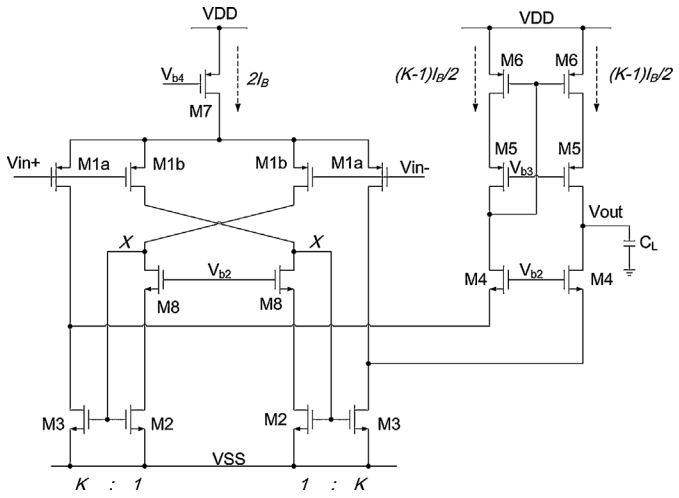

Fig. 1. The conventional RFC amplifier.

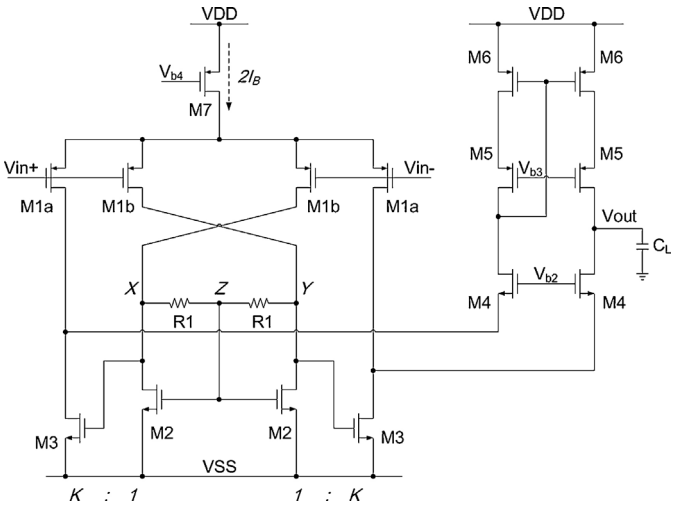

Fig. 2. The proposed CFRFC amplifier.

consequently the GBW of the RFC is [3,4],

$$GBW_{RFC} = \frac{(K+1)g_{m1a}}{C_L} \tag{2}$$

where C_L is the load capacitance. Owing to the enhanced transconductance, its dc gain is also improved. Meanwhile, the slew rate (SR) of RFC is also given as [3,4],

$$SR_{RFC} = \frac{2KI_B}{C_L} \tag{3}$$

where $2I_B$ is the bias current of input pairs. Therefore, in order to obtain a higher slew rate and GBW, the enhancement factor K must be larger. However, an increase in K leads to not only the same increase in power consumption, but also larger parasitic capacitances at node X, reducing the phase margin. The non-dominant pole at node X can be described as [4]

$$\omega_X = \frac{g_{m2}}{(K+1)C_{gs2}} \tag{4}$$

where C_{gs2} is the gate-to-source capacitance of transistor $M2$. Thus, the value of K should not be too large, and a reasonable value is set to 3. For this reason, the GBW and SR of RFC is twice and three times that of conventional FC counterpart with the same power dissipation.

3. The proposed CFRFC amplifier

The proposed OTA based on the local common-mode feedback structure (CFRFC) is shown in Fig. 2 where all transistors operate in the saturation region. The active current mirror load of input pairs $M1b$ are substituted by the local feedback loops composed by matched resistors $R1$. The common-mode drain voltages of transistor $M2$ are fed back to their gate terminal. In quiescent conditions, no current flows through resistors $R1$, and voltage at node X, Y equals that at node Z, which can be given as,

$$V_X = V_Y = V_Z = V_{THN} + \sqrt{\frac{I_B}{\beta_2}} \tag{5}$$

where V_{THN} and β_2 are the threshold voltage of NMOS transistor and transconductance factor of $M2$. Thus, the ratio of quiescent current I_Q through $M2$ and $M3$ is set by their W/L size ratio,

$$\frac{I_{Q,M3}}{I_{Q,M2}} = \frac{(W/L)_{M3}}{(W/L)_{M2}} \tag{6}$$

Note that if this ratio factor is chosen to be K, the power consumption is the same as that of RFC.

3.1. Transconductance and GBW improvement

For small signal analysis of the proposed CFRFC OTA, ac current would go through $R1$ and node Z becomes virtual ground. Thus, the expressions for equivalent transconductance (G_m) can be given as

$$G_{mCFRFC} \cong (1 + g_{m3}(r_{ds1b} \| r_{ds2} \| R_1))g_{m1a} \cong (1 + g_{m3}R_1)g_{m1a} \tag{7}$$

where r_{ds} is drain–source resistance of transistors. With a large value of R_1, $g_{m3}R_1$ would be larger than K, which leads to a significant boost in transconductance compared to the conventional RFC at the same quiescent power conditions. Also, the GBW of the proposed CFRFC are expressed as follows

$$GBW \cong \frac{(1 + g_{m3}R_1)g_{m1a}}{C_L} \tag{8}$$

where C_L represent the load capacitance at the output node. Note that due to increased transconductance, the enhancement of GBW is also obtained.

3.2. DC gain enhancement

The output equivalent resistance (R_{out}) of the proposed CFRFC can be given as follows,

$$R_{out} \cong [(g_{m5}r_{ds5})r_{ds6}] \| [(g_{m4}r_{ds4})(r_{ds3} \| r_{ds1a})] \tag{9}$$

Note that the output impendence of CFRFC is the same as that of RFC counterpart. And then the dc open-loop gain can be described as,

$$A_{dc} \cong (1 + g_{m3}R_1)g_{m1a}R_{out} \tag{10}$$

It is noticed that due to the improved transconductance, the dc gain of the proposed CFRFC is accordingly enhanced.

3.3. Slew rate boost

The large signal response of CFRFC can be analyzed as follows. Assume that a large positive step applied to V_{in+}, the input differential pairs $M1a$ and $M1b$ in left side will be cut off, and then voltage at node Y decreases, forcing transistors $M2$, $M3$ and $M4$ in the right side turn off. Due to transistor $M3$ in the right side is cut off, the input transistor $M1a$ in the right side goes into triode region. The tail current $2I_B$ enters into $M1b$ in the right side. Because of the local common-mode feedback, half of tail current flow through $R1$, and the other half goes into $M2$. Therefore, the maximum voltage swing