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ORIGINAL PAPER

Design of the FPGA-based gigabit serial link for PandaX-III prototype TPC

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Abstract
Background: PandaX-III is aimed to search for neutrinoless double beta decay of ^{136}Xe at China Jinping Underground Laboratory. To test various design features of PandaX-III detector, a prototype TPC with 20 kg Xe containing inside is built.
Purpose: Front-end boards installed inside the waterproof vessel integrate charge of Micromegas signal, digitize signal waveform and send data packet to back-end board. Front-end boards receive synchronous information (global clock, global trigger, etc.), as well as command messages from back-end board. In order to satisfy the requirement of high data throughput and multiple types of synchronous data transmission, we propose an optical fiber link to communicate between front-end board and back-end board.
Methods: Communication of serial transmission is performed using FPGA-based gigabit transceiver with a 1 Gbit/s point-to-point speed. A dedicated user-defined protocol is implemented for various kinds of data transmission.
Results: To validate the performance of this link, bit error rate and eye diagram were tested. Preliminary joint test with detector was conducted in Shanghai. All test results showed sufficient data bandwidth and stable performance.
Conclusion: To satisfy the requirement for data transmission between front-end board and back-end board in PandaX-III TPC detector readout, an FPGA-based gigabit serial link is designed and tested. This design shows good performance and will be applied to the R&D of PandaX-III TPC.

Keywords Gigabit transceiver · TPC · Micromegas · PandaX-III

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Introduction

PandaX-III experiment

Particle and Astrophysical Xenon experiment III (PandaX-III) is the neutrinoless double beta decay (NLDBD) detection experiment in China Jinping Underground Laboratory (CJPL) [1]. This experiment targeting to discover the rare nuclear weak decay could uncover the possible Majorana nature of neutrinos and thus would be an important breakthrough in fundamental physics [2]. The gas TPC technology for NLDBD provides high energy resolution and the capability of track detection, which is critical for identifying NLDBD events. Figure 1 shows the schematic of PandaX-III TPC. PandaX-III TPC is shielded by ultra-clean water in all directions to reduce background. Digitized signal data of front-end board need to be transferred back to back-end board and then to PC farm running software. One critical requirement of this readout scheme is to design an appropriate link between electronics, which needs high throughput, low material, water proof and robustness. The development of modern communication technology has offered optical fiber as a mature technology for high-speed, simple, waterproof and reliable data transmission. This paper describes the design of gigabit optical fiber link for PandaX-III prototype TPC.

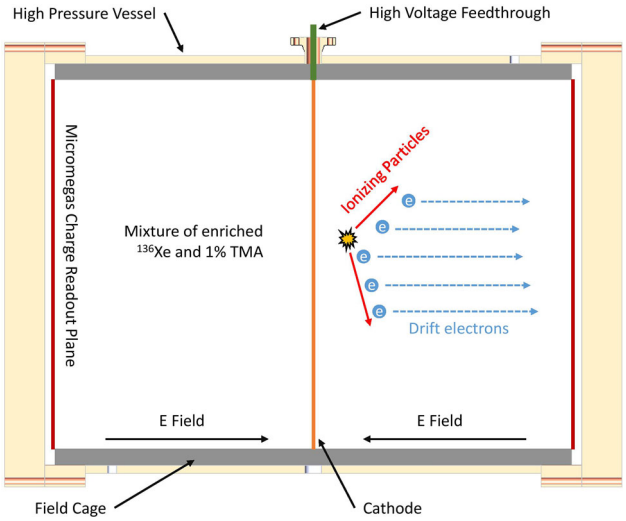

Fig. 1 Schematic of the PandaX-III TPC

Requirement of serial data transfer

In the current design, front-end card (FEC) is designed with 256 readout channels, covering 2 Micromegas modules. Each FEC contains 4 ASIC chip AGETs, each in charge of amplifying, shaping and 512 analog sampling for 64 channels. Besides, a discriminator for multiplicity building and self-trigger is provided in it [3,4]. Sampled analog signal from AGET is digitized by an ADC, and then the digitized waveform is processed in an on-board FPGA, and finally sent back through optical fiber.

According to Monte Carlo simulation, in PandaX-III experiment the trigger rate is at about 10-Hz trigger rate, event data rate of each FEC is about 21 Mbps. Considering the possibility of significant higher event rate in calibration runs, 1-Gigabit data bandwidth is necessary for FEC data transmission.

To realize a complete 3D track reconstruction, synchronizing clock and trigger of all FECs is necessary. A feasible way to realize global clock and trigger is using clock and trigger from the same source. FECs recover clock from serial data and generate clocks for ADCs and AGETs. Triggers from all FECs would be assembled by back-end board to generate global trigger, which then get distributed via optical fiber.

Realization of gigabit serial link

Design of serial link

To implement gigabit serial link that satisfies requirement of sending synchronous clock and trigger, configuration command and raw data simultaneously, we use FPGA-based high-speed transceiver, GTP on FEC and GTX on back-end DAQ board, respectively. The two boards use a 1310- and 1490-nm wavelength single-mode optical fiber as bidirectional communication medium. 1-Gbps small form-factor pluggable (SFP) optical transceiver module (MTBS1334L1CNN) transforms optical signal to high-speed serial data, and then these serial data are sent to FPGA. GTP/GTX integrated in FPGA is responsible for descrambling data, 8B/10B encoding and clock recovery. To accommodate requirement for decoding various type of data, we developed a user-defined protocol. When no valid data are transmitting, K28.5 (a specific control K character) is sent. The high 8-bit of the first valid data is used as the header of data package (currently 8'h0, 8'h1 and 8'h4 are indicators of trigger, command and payload data). The valid data followed after header are contents of package. Synchronized trigger package contains trigger bit, trigger type and time stamp. Sub-trigger is generated from AGET of FEC and then sent through fiber link to DAQ. DAQ board congregates multiple sub-triggers and uses FPGA trigger decision logic to generate a global trigger. This global trigger is fanout through optical

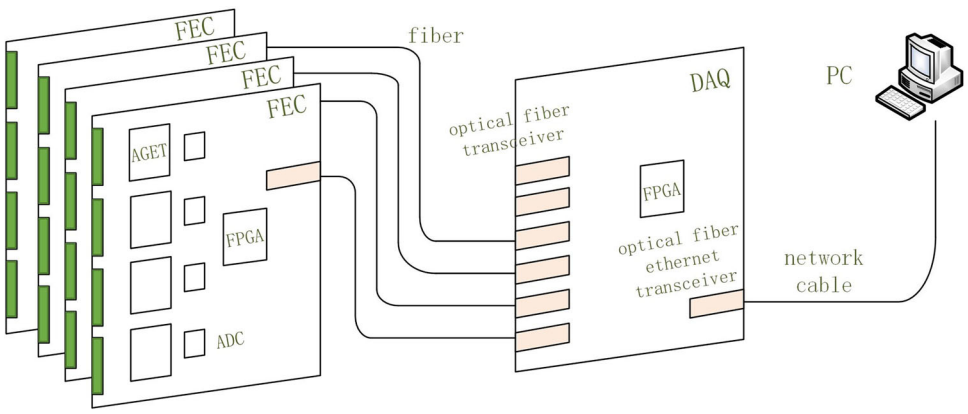

Fig. 2 Schematic block diagram of readout electronic system for prototype TPC

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