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An efficient ternary serial adder based on carbon nanotube FETs

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ABSTRACT

This paper presents an efficient ternary serial adder for nanotechnology employing negative, positive and standard ternary logics. Multiple-valued logic results in chips with more density, less complexity and high-bandwidth data transfer. The unique properties of CNTFETs such as the capability of adapting the desired threshold voltage by changing the diameters of the nanotubes and same carrier mobility for the n-type and p-type devices play an important role in designing this circuit. The proposed design method considerably reduces the number of required devices of a ternary serial adder. In addition, the results of the simulations conducted using HSPICE with the Stanford comprehensive 32 nm CNTFET model, demonstrate improvements in terms of speed and power-delay product as compared to the cutting-edge CNTFET-based ternary designs.

1. Introduction

Complementary metal oxide semiconductor (CMOS) is the main technology of the past decades that provides the satisfactory dimension scaling in order to achieve energy-efficient and high-density very large scale integration (VLSI) circuits [1]. However, scaling down the feature size of CMOS devices in nanometer regime results in challenges such as short-channel effects and reduced gate control. These problems can obstruct the consecutive dimension scaling of the CMOS technology and consequently reduces its appropriateness for the prospect high-speed, energy-efficient high-density applications [2]. Basic limitations of CMOS technology and expectations of Moore's law have prompted scientists to find a convenient alternative for this apparatus.

In order to overcome the aforementioned limitations, researchers try to develop other nanotechnologies such as silicon nanowire transistors, single electron transistor (SET), quantum-dot cellular automata (QCA) and carbon nanotube field effect transistors (CNTFET) [1–4]. Due to the remarkable properties of CNTFET, it seems to be a promising successor for CMOS among the various introduced alternatives. The similarities between the substructure of the conventional MOSFET and CNTFET make CNTFET a more feasible nanodevice for use in the structures designed based on CMOS without making any major changes. Moreover, because of the unique one-dimensional band structure of CNTFET, which suppresses backscattering and causes near-ballistic operation, CNTFET represents a very high-speed operation [5]. Considering higher performance, higher carrier velocity, higher transconductance and lower power consumption, CNTFET significantly illustrates greater performance than conventional CMOS transistors.

On the other hand, unlike the binary logic, there are more than two authorized logic levels in MVL systems so logical and arithmetic operations can be performed on more than two logic values. As a result, in MVL many logical and arithmetic operations could be executed with higher speed and smaller number of computation stages [5]. In addition, the most suitable method for designing voltage-mode MVL circuits is multiple-threshold (multi-V_t) design method and the desired threshold voltage can be achieved by setting the diameters of the nanotubes in CNTFET devices [4–7]. Considering the fact that in a typical binary VLSI chip almost 70% of the chip area is dedicated to the interconnects, 20% to the insulation, and just 10% to the device itself, it is not irrational to claim that diminished space on VLSI chips restricts the performance of binary logic [8]. Multiple-value logic can lead to increased data processing capability per unit area, reduced number of interconnections, as well as reduced number of active devices inside a chip, as compared to the binary logic. MVL modules have been applied to binary logic ICs to improve the performance of CMOS technologies. For instance, employing an efficient MVL implementation for a signed 32-bits multiplier compared to its fastest binary equivalent can lessen chip area and power consumption more than 50% [6]. Moreover, by utilizing multiple-valued logic, serial and serial–parallel arithmetic operations can be carried out faster [5].

Considering different MVL systems, using radix e ($e = 2.718\ldots$) results in the most efficient design of the digital systems. Nevertheless, because of the restriction on hardware implementation, designers are restricted to use natural numbers as the bases for

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calculations. As a result, the most efficient MVL system, which results in lower cost and complexity than binary, is the ternary logic [9].

Full Adder is definitely the most important circuit among the various processing elements used in a microprocessor. Performance improvement of signal processors mainly depends on the development of adder circuits. Therefore designing an efficient CNTFET-based quaternary full adder cell supporting all the possible logic values for the near future non-silicon non-binary integrated circuits and systems can be more of an interest.

Full Adder is definitely the most important arithmetic module used in a microprocessor. Hence, performance improvement of signal processors mainly depends on the development of efficient adder circuits. In addition, serial addition can be better for low-energy applications and leads to a considerable hardware efficiency.

According to the aforementioned discussions, designing an efficient CNTFET-based ternary serial adder for the near future non-silicon non-binary integrated circuits and systems can be more of an interest. In this paper, an efficient ternary serial adder is proposed using CNTFET.

The rest of the paper is organized as follows: Sections 2 and 3 briefly review the CNTFET nanodevice and ternary logic, respectively. The proposed design is described in Section 4. Section 5 includes the simulation results and finally Section 6 concludes the paper.

2. A brief overview of the CNTFET nanodevice

Carbon Nanotube (CNT) was discovered in 1991 by S. Iijima. CNT is a nano-scale tube which is made up of rolled sheet of graphene. CNT falls into two categories, multi-wall (MWCNT) and single-wall (SWCNT). A MWCNT is composed of more than one cylinder while a SWCNT is a single cylinder. A SWCNT could be a semiconductor or a conductor, depending on its chirality vector. The chirality vector is the wrapping vector that the graphene sheet is considered to be rolled up along and is defined by (n_1, n_2) indices. They determine the arrangement angle of the carbon atoms along the nanotube. If $n_1 - n_2 \neq 3k$ ($k \in Z$), the SWCNT is a semiconductor and otherwise it is metallic. Semiconducting SWCNTs can be used as the channel of the CNTFET device [10–12]. Fig. 1a illustrates a general structure of a CNTFET device.

Unlike the silicon MOSFET, p-type and n-type CNTFETs have the same carrier mobility ($\mu_n = \mu_p$) and hence the same drive current capability [10]. This unique characteristic of the CNTFET device is very significant for simplifying the design and transistor sizing procedures of complex CNTFET-based circuits.

Another great advantage of the CNTFET nanodevice in comparison with the nanoscale MOSFET is its I–V characteristics which are similar to well-tempered classic MOSFET devices. In addition, similar to a MOSFET, a CNTFET also has a threshold voltage, which is the voltage required for turning on the device via the gate. Adapting threshold voltage of a CNTFET just by changing the diameter of its CNTs makes it more flexible than MOSFET for designing digital circuits and also very appropriate for designing multi-V_t circuits. The threshold voltage of a CNTFET is approximately considered as the half bandgap and can be calculated by equation (1) [10].

$$V_{th} \simeq \frac{E_g}{2e} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \simeq \frac{0.43}{D_{CNT}(nm)} \tag{1}$$

where a (≈0.249 nm) is the carbon to carbon atomic distance, V_π (≈3.033 eV) is the carbon π–π bond energy in the tight bonding model, e is the unit electron charge and D_{CNT} is the diameter of CNTs, which is calculated by equation (2) [10].

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \simeq 0.0783\sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{2}$$

It can be inferred from equations (1) and (2) that by changing the diameter and the wrapping vector of a CNT, which is defined by its chirality indices (n_1, n_2), the bandgap of CNT and threshold voltage of CNTFET can be modified.

It is worth pointing out that various useful and operational solutions have already been presented in the literature for growing CNTs with a defined chirality and implementing the desired threshold voltage for multi-tube CNTFETs [13–15].

Three distinct forms of CNTFET devices have been already introduced in the literature. Schottky Barrier (SB) CNTFET is the first one (Fig. 1b), a tunneling device operating in the rules of direct tunneling through a SB at the source–channel junction. Due to its fabrication, which uses direct contact between the semiconductor CNT and the metal, it has a SB at the CNT–metal junction that causes

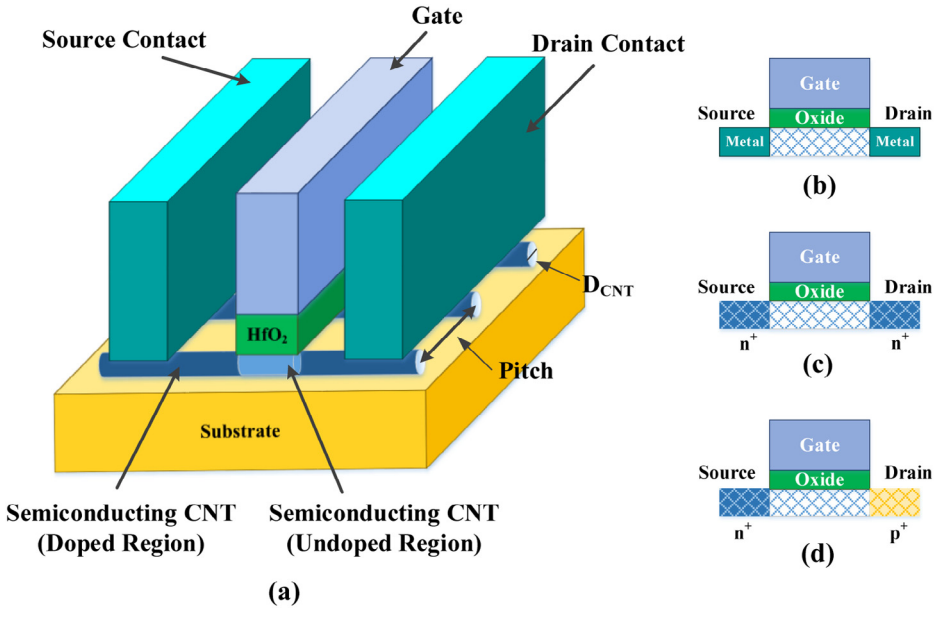

Fig. 1. CNTFET. (a) Detail structure of MOSFET-like CNTFET. (b-d) Three different types of CNTFET.