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Low voltage high performance hybrid full adder

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ABSTRACT

This paper presents a low voltage and high performance 1-bit full adder designed with an efficient internal logic structure that leads to have a reduced Power Delay Product (PDP). The modified NOR and NAND gates, an essential entity, are also presented. The circuit is designed with cadence virtuoso tool with UMC 90-nm and 55-nm CMOS technologies. The proposed adder is compared with some of the popular adders based on power consumption, speed and power delay product. The proposed full adder cells achieve 56% and 76.69% improvement in speed and power delay product metric when compared with conventional C-CMOS full adder. It is also found that the proposed adder cells exhibit excellent signal integrity and driving capability when operated at low voltages.

1. Introduction

The explosive growth of battery operated portable applications such as cellular phones, smart cards, PDAs, laptops and the evolution of the shrinkage of the technology requires smaller silicon area, high throughput circuitry and most importantly low power [1–3]. Power consumption of any system can be reduced by scaling the supply voltage and operating frequency. But, it increases the propagation delay of the system and degrade the driving capability of the design [4,5]. Therefore, designing a full adder with improved power delay characteristics is of great interest.

Digital Signal Processing (DSP) is an important unit in electronic devices. DSP based processors are used to perform the operations such as video processing, filtering and fast Fourier transform (FFT). Such modules perform extensive sequence of addition/subtraction, multiplication and division computations. Addition is the most fundamental operation in arithmetic circuits [6,7]. Full adders are encountered in the critical path of the complex arithmetic circuit like multiplication, division and address calculations [8–13]. These are the core elements of any system and can significantly influence the performance of any system. That is why enhancing the performance of the 1-bit adder cell can enhance the overall system performance [11,14,15].

Several logic styles have been used in the past to implement the full adder cell. Each logic style has its own advantages and disadvantages. Standard static CMOS full adder (C-CMOS) is based on regular CMOS structure with pull up and pull down transistors. This adder provides full output voltage swing against voltage and transistor sizing. The limitations of this design are its larger area and slower speed due to the availability of PMOS devices and larger input capacitance of the static CMOS logic gates [16]. On the other hand, complementary pass transistor logic (CPL) is fast and also provides full voltage swing output [17]. CPL adder is based on dual rail structure and requires 32 transistors. But it has larger power consumption because of the presence of static inverter and lot of internal nodes [18,19]. The other adders are designed using hybrid logic styles and are called hybrid adder. These adders are designed with a combination of more than one logic style to enhance the overall performance of the system. The main focus of hybrid logic style is to reduce the number of transistors and power dissipating nodes of the adder cell. Hybrid pass logic with static CMOS (HPSC) is an example of hybrid adder. HPSC provides full output voltage swing and has good output drive capability. The limitation of this adder is its higher propagation delay [20]. On the other hand, hybrid adder is a good choice in terms of power consumption and speed than HPSC but at the cost of increased number of transistors in the design [21]. However, hybrid CMOS full adder is faster than HPSC at all supply voltages. But its delay is increased with varying the load [1].

Full adder proposed in Reference 2 is designed with less transistors and consumes lesser amount of power. But it fails to provide full swing output voltage when operated at low voltages. This results into deteriorated signals and degradation in speed tremendously with the scaling of the supply voltage. In this adder, signals have higher rise and fall time at lower voltages and it makes the design inefficient at the scaled technology.

The internal logic structure based on transmission function theory is proposed in Reference 22 to build the full adder cell as shown in Fig. 1. It consists of three main blocks to obtain the sum and carry

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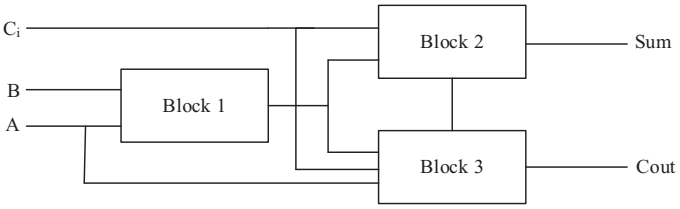

Fig. 1. Full adder module based on three logic blocks.

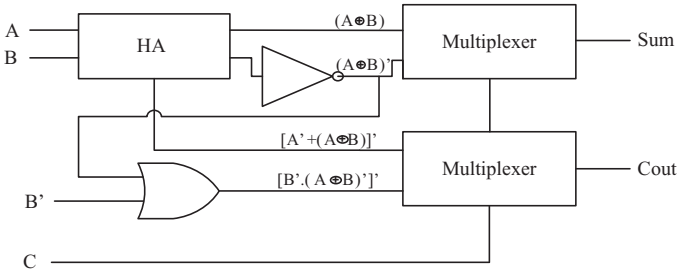

Fig. 2. Proposed internal logic structure for designing the 1-bit full adder cell.

outputs. Block 1 has XOR/XNOR gate to generate $(A \oplus B)$ and $(A \oplus B)'$ signals and block 2 and block 3 are used as XOR blocks or multiplexers to obtain the sum and carry outputs. This structure has been adopted by many researchers as a standard structure for designing the 1 bit full adder cells. Some of the popular designs are described in References 18,23–25. But the major problem of the module reported in Reference 22 is the presence of intermediate signals $(A \oplus B)$ and $(A \oplus B)'$ [26,27]. These intermediate signals are used to drive the output blocks or multiplexers and therefore responsible for higher propagation delay and power consumption.

To reduce the overall propagation delay and power consumption a new full adder cell is designed with internal logic structure. The proposed structure uses inputs signal C and its complement C' to drive the output multiplexers in place of the intermediate signal $(A \oplus B)$ and its complement $(A \oplus B)'$. The logic structure designed with input signal C also helps in reducing the overall hardware cost of the design. This logic structure consists of XOR/XNOR gates, modified NOR and NAND gates with multiplexers inserted at the output. Multiplexers are used to select the sum and carry outputs. The resultant full adder exhibits improved PDP compared to earlier reported adder designs. Proposed design also has full output swing and is found suitable when operated at lower voltages.

The rest of the paper is organized as follows. Section 2 introduces the proposed internal logic structure to build the 1-bit high speed full adder cell. Section 3 describes simulation test bench. The simulation results and comparison of the entire referred and proposed full adder cells are presented in section 4. Voltage and temperature analysis of the proposed design is carried out in section 5. Section 6 draws the conclusion.

2. Implementing 1-bit full adder with proposed internal logic structure

In the proposed structure, the selection of sum and carry outputs are made under the control of input signal C. This signal is not generated internally and therefore provides full output voltage swings with no additional delay. It has good driving capability and used to drive the multiplexers at the output of the full adder cells. Based on this logic structure and using Swing Restored Complementary Pass transistor Logic (SR-CPL) new full adder is proposed. The block diagram of the proposed 1 bit full adder designed with internal logic structure is shown in Fig. 2. It is designed after analysing the truth table of full adder cell as shown in Table 1. The transistors schematic of the proposed design is shown in Fig. 3.

Table 1
Truth table of 1-bit full adder.

A	B	C	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

In Fig. 3(a.1–a.3) three basic CMOS inverter are shown which gives the complement output of the input signals A, B and C in the form of A' B' and C' respectively. Similarly Fig. 3(b) represents the SR-CPL based XOR gate and its complement in the form of XNOR gate. A and B are the input signals applied on these gates. In Fig. 3(c) and (d) modified NOR and modified NAND gates are shown. Multiplexers required for generating the sum and carry outputs are shown in Fig. 3(e.1) and (e.2). Transmission gates are used for designing the multiplexers. The proposed full adder cell is realized using the logic structure of Fig. 3.

The modified NOR and modified NAND gates "as essential entities" are also proposed and shown in Fig. 3(c) and (d). A' and $(A \oplus B)$ are the inputs applied on NOR gate and outputs are shown in the form of $[A'+(A \oplus B)]'$. Similarly B' and $(A \oplus B)'$ are the inputs applied on NAND gate and output are shown in the form of $[B'.(A \oplus B)']'$. Due to this input combinations proposed NOR and proposed NAND gates require only three transistors. This makes the proposed design faster, compact and power saving. The operation of the modified NOR and NAND gates are described in Tables 2 and 3 respectively. The output combinations of these gates are selected by the output multiplexers to generate the final carry output.

After analysing the logic structure, it is obvious that Sum output is equal to $(A \oplus B)$ when C is 0 and becomes equal $(A \oplus B)'$ when C is 1. Similarly, carry output is equal to $[A'+(A \oplus B)]'$ when C is 0 and becomes equal to $[V'.(A \oplus B)']'$ when C is 1. Therefore, this optimized structure successfully operates under the control of input signal C. Hence, the proposed logic approach is faster due to the presence of signal C. This signal reduces the overall delay and power consumption of the proposed designs. In addition to this, the capacitive load of this signal C is also reduced as it is connected only to some transistor gates. Reductions in power consumption and propagation delay further improve the PDP of the proposed adder as compared with existing adders. Power consumption and propagation delay can be minimized further by sizing the XOR/XNOR,

Table 2
Truth table of modified NOR gate.

A'	$(A \oplus B)$	$[A'+(A \oplus B)]'$
0	0	1
0	1	0
1	0	0
1	1	0

Table 3
Truth table of modified NAND gate.

B'	$(A \oplus B)'$	$[B'.(A \oplus B)']'$
0	0	1
0	1	1
1	0	1
1	1	0