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ScienceDirect

Procedia Computer Science 86 (2016) 184 – 187

Procedia Computer Science

2016 International Electrical Engineering Congress, iEECON2016, 2-4 March 2016, Chiang Mai, Thailand

Current Differencing Transresistance Amplifier (CDTRA) and Its Application for Analog Signal Processing

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Abstract

This article presents a design of current differencing transresistance amplifier (CDTRA). It can be controlled of output voltage gain by R_m. The output terminals offer both in current and voltage signals. Furthermore, the circuit is theoretically temperature-insensitive which is preferable to use in a temperature variation work. The PSpice simulation results confirm the CDTRA. In addition, an application in a grounded inductance simulator is disclosed. The total power consumption is 3.53mW at ±3V power supplies.

Peer-review under responsibility of the Organizing Committee of iEECON2016

Keywords: Current Differencing Transresistance Amplifier, Grounded Inductance Simulator

1. Introduction

In the past, an integrated circuit design by using op-amp is used widely in analog signal processing. However, these reported circuits suffer from the limitation caused by the finite gain-bandwidth product and limited slew rates, it is not preferable to used for higher frequencies.

In 1992, a reported 3-terminals active element namely operational transresistance amplifier (OTRA)[1]-[5], it is a high gain current input voltage output analog building block, the input and output terminals are characterized by

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Peer-review under responsibility of the Organizing Committee of iEECON2016
doi:10.1016/j.procs.2016.05.056

low impedance, thereby eliminating response limitations incurred by RC time constants. The input terminals of the OTRA are virtually grounded, so the effect of parasitic capacitances and resistances at the input is disappear. Thus, the OTRA can work in high frequency. Unfortunately, the output offers only in voltage, so it limits the flexibility of applications.

The purpose of this paper is to realize of current differencing transresistance amplifier (CDTRA). The features of proposed circuit are that: high gain and high bandwidth are obtained, and the amplitudes can be linearly controlled via R_m, the circuit description is very simple; it can provide both current and voltage signals. Its performances are illustrated by PSpice simulations they show good agreement as mentioned.

2. Basic concept of CDTRA

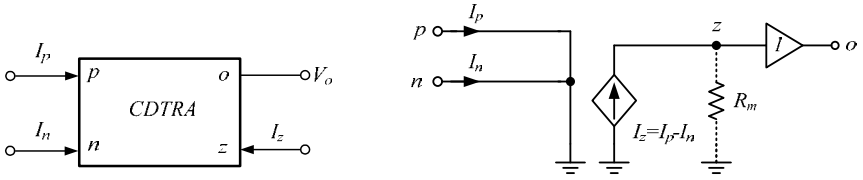
The CDTRA is a 4-terminal building block, shown symbolically in Fig. 1 and its port relations are characterized by the matrix equation

$$\begin{bmatrix} V_p \\ V_n \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ R_m & -R_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_z \\ I_o \end{bmatrix}, \tag{1}$$

where R_m is the transresistance gain, I_p and I_n are the input current, V_o is the output voltage.

In CDTRA, both the input terminals are virtually grounded and the output voltage is the difference of the two input currents multiplied by the transresistance gain R_m, such that

$$V_o = R_m(I_p - I_n)\,. \tag{2}$$



(a) (b)

Fig. 1. The CDTRA (a) symbol (b) equivalent circuit

3. Proposed CDTRA

The proposed realization of the CDTRA is shown in Fig. 2. The circuit consists of a current differencing circuit: $Q_1 - Q_{11}$ and the buffered output of O terminal uses transistors: $Q_{12} - Q_{15}$. The output current at Z terminal is a total of current difference between I_p and I_n.

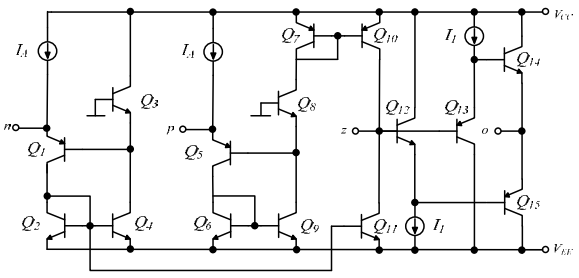


Fig. 2. Internal Construction of the CDTRA

4. Simulation Results

To prove the performance of the CDTRA, the PSpice simulation program was used. The PNP and NPN transistors employed in the proposed device were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T [6], biased with ±3V supply voltages. Fig. 3 displays DC transfer characteristic of the CDTRA, when $R_m = 1k\Omega$. So it is seen that it is linear in