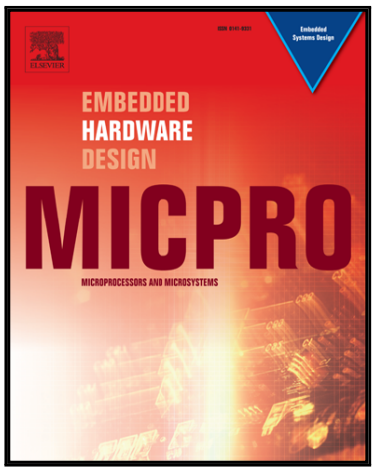

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Low-Power and High-Speed Shift-Based Multiplier for Error Tolerant Applications

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***Abstract* — We propose a new multiplier design that fulfills the need for low-power circuit blocks used in error-tolerant applications on energy-constrained devices. The design trades accuracy for higher speed, lower energy consumption, and lower transistor count. The average relative error of an *N*-bit multiplier is modeled as a function of *N* and saturates at a constant (around 17%) as the multiplier width increases. An 8-bit implementation simulated in HSPICE achieved almost 90% energy savings for a random sample of operands as compared to a conventional parallel multiplier. The design is flexible whereby simple variations to the circuit structure lead to a perfectly accurate multiplier. Tests performed on multimedia applications such as JPEG compression showed a promising outcome.**

Keywords: multiplier, error-tolerant applications, low power, error model, shift-and-add, pass transistor logic, integrated circuits.

I. Introduction

With the advances in transistor technology and parallel computing, energy consumption has become the new major hurdle, especially for energy-limited devices such as smartphones and other portable devices. Today, the need for energy aware computing is more than ever. Many approaches aim to fulfill this need on the transistor, circuit, architecture, and device levels [1].

In this paper, we target error tolerant applications [2] and focus on designing a stochastic low-power multiplier block, given that the multiplier is extensively used in very important applications such as digital signal processing. Even though stochastic circuit blocks produce inaccurate results, they should not deteriorate the user experience or the main function of the application. We exploit in this paper the error tolerance of these applications to significantly improve the speed, performance, power, chip area, and energy consumption of the multiplier block. The proposed multiplier can for instance be a building block in the stochastic ALU of the general-purpose hybrid processor architecture discussed in [1].

We propose a new multiplication scheme that looks promising in achieving our aims. We compute its maximum error and model its average error in terms of the width of the multiplier. Many variations of our scheme are provided to show the flexibility of the design. Also, we propose two different designs for our scheme and then simulate them and validate their benefits. Finally, we test the scheme on a JPEG encoding algorithm to demonstrate its feasibility in error-tolerant multimedia applications.

The rest of the paper is organized as follows: Section II discusses related work. Section III discusses our proposed multiplier scheme along with its variations. Section IV presents the design and implementation of our multipliers. Simulation and testing results are presented in section V. We conclude and present potential future work in section VI.

II. Literature Review

M. Mottaghi-Dastjerdi et al. [3] state that the generation of partial products, i.e. the repeated shifts and additions that converge to the accurate result, is the largest contributor to the total power consumed in shift-and-add multipliers. The authors propose a new low-power structure for shift-and-add multipliers that can be used for low-power applications that do not primarily depend on speed. It is different from the conventional multiplier where multiplying A by B includes directly feeding A to an adder, bypassing the adder when possible, using a ring counter instead of a binary counter, removing the partial product shift, and eliminating shifting the B register. Simulation results showed that the proposed architecture lowers the total switching activity to 76% and the power consumption to 30% compared to the conventional case.

V.Muralidharan and M.Jagadeeswari [4] propose a new type of adder that achieves high performance while attaining low power consumption for digital signal processing applications. They target the addition operation by eliminating the carry propagation path, which accounts for the major portion of the energy consumption of the adder block in the conventional ripple carry adder in addition to a large contribution to the adder delay.

The authors of [5] propose an innovative multiplication scheme where the operands are split and only their most significant parts are multiplied accurately while the other parts are approximated by simple logic. The resulting errors are considered acceptable for circuit designers and users. This scheme proved to enhance the speed and to reduce the power consumption.