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A versatile architecture for long-term monitoring of single-event transient durations

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ABSTRACT

We present design and analysis of an on-chip measurement infrastructure, which facilitates long-term monitoring of single-event transient durations in digital VLSI circuits exposed to uncontrollable radiation. Unlike the known oscilloscope-based methods, our approach is all-digital: SET durations are measured by the SET-gated counting of pulses generated by a high-frequency ring oscillator, and stored in an up/down-counter array organized in a ring. We carefully elaborate a comprehensive concept for making our infrastructure SEU tolerant, with the main challenge being to attain a sufficiently high probability of recording useful hits in the target before exhausting the SEU tolerance of the infrastructure. Our key contribution here concerns the protection of the counter array: Rather than resorting to radiation hardening or explicit triple modular redundancy (TMR), we save area by using a novel redundant duplex counter architecture: For a small number of recorded SETs, our architecture implicitly implements TMR, albeit in a way that degrades gracefully for larger numbers of recorded SETs. Besides standard functional and timing verification, we use Spice-based SET injection for verifying the effectiveness of our SEU-tolerant architecture, and some cross section-based probabilistic analysis for confirming that our measurement infrastructure based on it indeed achieves its purpose.

1. Introduction

Due to the steadily decreasing feature sizes of modern VLSI circuits, which are in the nanometer range nowadays, *single-event effects* (SEE) are increasingly dominating the fault rate of VLSI circuits [1–7]: SEEs occur when active areas of a VLSI circuit, namely junctions of transistors, are hit by ionizing particles. Such particles primarily originate in high-energy cosmic radiation, either directly (at high altitudes, i.e., in space and aerospace) or indirectly, via interaction with the atmosphere. Furthermore, they may be created inside the ASIC, via nuclear interactions of atmospheric neutrons with silicon.

Unlike permanent SEEs such as latch-up, threshold voltage shifts and even destructive burn-outs in power semiconductors [8–10], the primary concern in modern VLSI circuits are *transient* SEEs: An ionizing particle hitting a junction of a transistor deposits charge along its track, which in turn can cause a *single-event transient* (SET) signal pulse (< 1 ns range) on the output. If the affected transistor is part of a storage element (e.g. an SRAM cell or a latch), this may cause the element to flip its state, thereby leading to a *single-event upset* (SEU). Unfortunately, SEUs may also occur if the hit transistor is part of combinational logic, since a sufficiently strong SET may propagate until it reaches a storage element where it is latched. In any case, however, the errors resulting from SEUs are not permanent but rather transient (i.e., can be corrected), and are hence called *soft errors* (SE).

Soft error rates (SER) increase primarily because of three reasons: (i) Increased circuit complexity results in more hit targets, (ii) decreasing feature sizes and supply voltages decrease the electrical charge used for representing information, which makes it more likely for a particle hit to create an SEE, and (iii) increasing clock frequencies increase the probability that an SET generated in combinational logic gates gets latched and hence causes an SEU.

Robust circuit design—in particular, for critical applications in space and aerospace, where ionizing particles are abundant—hence needs models that accurately describe SET/SEU generation and propagation in modern VLSI technology, yet are easy and efficient to use at early design stages: Such models both allow to assess the radiation tolerance of different architectural designs and hardening techniques, and to estimate the final soft-error rate of a circuit.

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Part of our related projects EASET and FATAL[1] are devoted to this problem.

This paper reports on an important milestone within this endeavor, namely the design of an on-chip infrastructure for SET pulse width measurements. Beyond providing an all digital solution for accurate timing measurements of pulse widths in the range of single ns, a key challenge was to develop an efficient solution for obtaining radiation tolerance for the measurement circuitry: Standard solutions like radiation hardening by sizing or triple modular redundancy are known to guarantee single fault tolerance, but they increase the area to the point where it is likely to experience multiple faults in the measurement circuitry (and hence exhaust the available radiation tolerance) before obtaining any correct SET pulse width measurement in the actual target circuit.

The subsequent section will provide more background on the aims and setup of our experiments and will hence make the challenges more comprehensible. Following Section 3, which contains an overview of related work, we list the features and requirements of our measurement infrastructure in Section 4. Section 5 then presents all the architectural details of our measurement infrastructure. Section 6 contains the results of our functional and SEU-tolerance analysis, Section 7 provides our probabilistic analysis. A discussion of our results in Section 8 and some conclusions in Section 9 round off the paper.

2. Setup for the radiation experiments

The overall target of our research projects FATAL and EASET is to develop a better understanding of the effect of particle hits in digital VLSI circuits in general. Besides on physical and electrical modeling, where TCAD and Spice simulations [3,11] are the primary method of validation, they also focus on novel approaches for experimental validation. Note that it is vital to have measurement results available that can serve as a ground truth when trying to improve state-of-the-art SET models (specifically, SPICE models), for example.

To this end, we designed two types of target ASICs for our experiments, both comprising (i) a set of fundamental circuit blocks that serve as actual radiation targets, and (ii) some on-chip measurement infrastructure. As our primary interest lies in the investigation of SET generation and electrical masking effects, rather than temporal and logical masking, we restricted our attention to relatively simple radiation target circuits, which can be considered worst case with respect to SET susceptability: Inverter, NAND, NOR, XOR, inverter chain, inverter tree, NAND-NOR tree, XNOR tree, Muller pipeline, flip-flop chain and Sklansky adder. Note that more complex target circuits would increase the overall RC of the circuit, thereby mitigating any minor particle strikes.

On our first type of ASICs, high-speed analog on-chip amplifiers plus an external real-time oscilloscope were used for the faithful measurement of SET pulse shapes occurring in digital 90 nm CMOS technology in micro-beam irradiation experiments [12,13]. This type of ASICs provides very precise information, but is, due to the significant size of the analog amplifiers, limited to the observation of few nodes in few and relatively small target circuits.

Our second type of ASICs has been first instantiated by a fully digital experimental chip that allows to study (on a larger scale) location, effect, rate, duration and propagation of SETs when exposed to radiation. To this end, we abandoned the analog amplifiers and placed an all-digital measurement infrastructure on chip instead, which collects and temporarily stores relevant data and periodically communicates it to an attached (off-chip) controller via a digital interface [14,15]. This makes our digital ASIC more flexible to use (for monitoring SET generation during oversea flights, for example) and allows monitoring significantly more target circuit nodes over longer periods to collect statistical data.

Unfortunately, though, our first version of the digital SET monitoring infrastructure, unlike the analog one, could not also determine the *duration* of the SET pulses. In the meantime, however, we developed a suitable measurement approach [16] based on SET-gated counting of the number of pulses of a very high-speed ring oscillator. Some of the key points of the resulting pulse-width measurement infrastructure, which is described in the present paper, are the following:

- For measuring the pulse widths, we always monitor the outputs of the respective target circuit, irrespective of size or type of the targets.
- We operate the target circuits in static mode, so output activity will only be triggered by a particle strike in a target. Therefore we can use any target circuits with this infrastructure, without having to consider how their dynamic operation interleaves with potential SETs.

For our experiments, we consider two types of radiation sources, namely a well controlled one like a micro beam [17], and an uncontrolled “ambient” one like a radiation chamber in a nuclear reactor. While the radiation can be confined to the target circuits alone with the former, the whole ASIC, including the measurement infrastructure, is exposed to radiation with the latter. Whereas our analog ASICs can be used with the micro beam only[2], our digital ASICs shall be fit for both. Clearly, to obtain meaningful experimental data under uncontrolled radiation, the measurement infrastructure must be made sufficiently radiation tolerant, in the sense that it is likely to observe target SET hits before the radiation tolerance of the measurement infrastructure is exhausted.

To accomplish this also in the new version of our digital ASIC (called FRad ASIC), we combine the above SET duration measurement with a novel SEU-tolerant on-chip counter architecture described in Section 5. The main challenge here originates from the fact that our target circuits are quite small in size. As all possible measures to increase their area would either change the (character of the) SET sensitivity of the circuit (e.g., when replacing single gates by chains, in which ultimately propagation effects are dominant), or decrease the quality of the measurement results (e.g., when ORing SET effects in parallel structures), our solution can live with the low ratio of the area of target and measurement infrastructure. Essentially, we require that the particle flux is small enough to ensure that there are not too many SEUs in the measurement infrastructure during a measurement period. Whereas this implies that it may take some time until a measurement period with a target SET hit is encountered, this is acceptable for our purpose: Since we target long-term experiments, we can afford to wait for this to happen, provided we can be sure that we will not erroneously interpret measurement infrastructure SEUs as target SET hits. The latter is circumvented, i.e., very improbable, by the SEU-tolerance properties of our architecture.

In addition to standard functional and timing verification of a detailed Spice model using Synopsis, we employed double-exponential SET injection [18] to verify the effectiveness of our

[1] EASET (Accelerator-based Experimental Analysis and Simulation Modeling of Single-Event Transients in VLSI Circuits) and FATAL (Fault-tolerant Asynchronous Logic) are/have been supported by the Austrian Science Fund (FWF) under project numbers P26435 and P21694. For more information, consult http://ti.tuwien.ac.at/ecs/research/projects/easet/ and http://ti.tuwien.ac.at/ecs/research/projects/fatal/. This paper was partly supported by the Austrian Science Fund (FWF) projects RiSE (S11405) and SIC (P26436).

[2] A second generation of our analog ASICs has recently been finalized, however, which provides some fault tolerance for the analog amplifiers as well. It might be suitable, to some degree, for the second type of ratiation sources also.