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A novel IP-core mapping algorithm in reliable 3D optical network-on-chips

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ABSTRACT

The Optical Network-on-Chip (ONoC) is considered as a promising way to achieve high performance of multiprocessor systems, and it will be a 3-Dimensional (3D) architecture organized by a certain topology where optical routers are optically interconnected with each other. For the design of 3D ONoCs, the highly reliable IP-core mapping is a key problem of properly assigning IP cores onto optical routers for a given communication task, and it has two main challenges: reliability estimation and mapping scheme. As for reliability estimation, crosstalk noise and thermal sensitivity which severely influence Signal-Noise-Ratio (SNR) should be measured. In addition, although standard genetic algorithms have been widely utilized to solve the optimal mapping solution due to the superiority of simple process, there are some deficiencies such as premature convergence and inferior local searching. In this paper, the impact factors of ONoC reliability are measured by SNR and thermal models, and we also design a novel IP-core mapping algorithm called as CGSA (Cataclysm Genetic-based Simulated Annealing) based on proposed models. In CGSA, we integrate genetic with an improved simulated annealing algorithm assorted with cataclysm strategies, in order to speed up the searching process. Furthermore, to enhance the network reliability, CGSA is bound with the topology selection, i.e., CGSA generates the optimal mapping solution with the best matched 3D ONoC topology. Simulation results show that CGSA is effective on achieving the higher reliability than benchmarks.

1. Introduction

The integration of many hardware functions and software routines on a single silicon chip becomes the development trend of electronic systems [1]. However, the Network-on-Chip (NoC) component has suffered from severe performance bottleneck in terms of high power consumption, transmission delay, and low bandwidth provisioning, as predicted by the ITRS roadmap. Therefore, the Optical Network-on-Chip (ONoC) is proposed as promising communication architecture for the future multiprocessor systems [2–4].

To systematically solve the problem caused by the bus architecture, ONoCs transplant computer network technology into the design of chips based on optical interconnections. Silicon photonics has become one of the most promising photonic integration platforms, which also promotes the development of ONoCs. Most importantly, the optical interconnection of silicon photonics has incomparable advantages of high bandwidth provisioning as well as low power dissipation and transmission delay. On the other hand, the 3-Dimensional (3D) integrated circuit is an attractive solution to overcoming the barriers to decreasing an interconnection scale [5]. To combine the advantages of optical interconnection and 3D integration, researchers proposed the concept of 3D ONoCs, i.e., a 3D architecture organized by a certain topology where optical routers are optically interconnected with each other. Compared with traditional 2D structures, 3D ONoC further reduces the physical connection length between a pair of chip lines, thus leading to the shorter transmission distance, the smaller transmission delay, and the lower power consumption [2–4].

IP-core mapping is a key problem when we design 3D ONoCs, and it has a significant influence on the network performance. IP-core mapping refers to the process of properly assigning IP cores onto optical routers for a given communication task. In general, IP-core mapping mainly contains two steps, as shown in Fig. 1. In step 1, the mapping solution generates using a mapping algorithm, and then it will be evaluated according to an estimation model in step 2, and feedback to step 1 for the solution optimizing adjustment [6]. Repeat two steps until the upper limit. Obviously, there are two main challenges of IP-core mapping in 3D ONoCs: mapping scheme and estimation model.

From the aspect of mapping schemes, genetic algorithms (GAs) were widely used to find mapping solutions for NoCs [7–9], but they merely considered a predefined topology and a single optimization objective. The authors in [7] proposed a multi-objective GA-based algorithm that not only jointly optimized power consumption, transmission delay, and chip area but also combined the optimal mapping solution with the topology selection. However, this approach is

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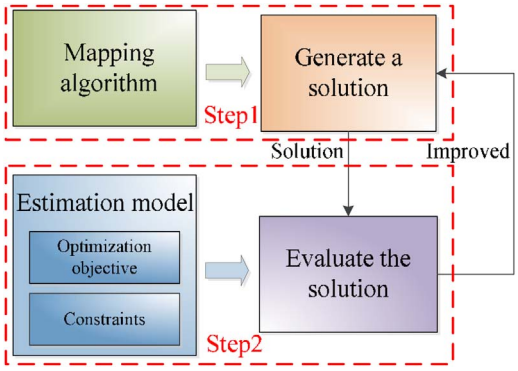

Fig. 1. IP-core mapping process.

confined in NoCs and cannot be extended into 3D ONoCs. Furthermore, standard genetic algorithms have two shortages when we solve an IP-core mapping problem: premature convergence phenomenon and inferior local searching.

Lots of researchers have designed accurate estimation models aimed at minimizing the power consumption and transmission delay for NoCs [10]. However, different from NoCs, the crosstalk noise and thermal sensitivity which severely influence Signal-Noise-Ratio (SNR) are intrinsic characteristics of photonic devices used by 3D ONoCs [11], and they should be taken into account for designing a novel reliability estimation model.

In this paper, we propose a methodology of finding the optimal IP-core mapping solution along with the best matched 3D ONoC topology, in order to ensure the high reliability. Our methodology includes three phases. Firstly, given a communication task graph, a novel mapping algorithm is designed to generate mapping solutions and their assorted 3D ONoC topology. Next, an original reliability model is proposed as the cost function of evaluating the reliability. Finally, we adjust the mapping solution according to evaluation results. Our contributions are summarized as follows.

1) To quickly search the mapping solution, a novel mapping algorithm based on the hybrid optimization strategy which combines improved GA and Simulated Annealing (SA) algorithm was proposed by us.
2) Used SA algorithm improves the ability of local exploration, and meanwhile, the cataclysm strategy applied to CGSA helps us jump out of the stagnation by generating new individuals.
3) An original reliability estimation model was designed to mathematically evaluate the 3D ONoC reliability from two aspects: crosstalk noise and thermal balancing.

The rest of this paper is organized as follows. Our reliability estimation model is in Section 2. Our Cataclysm Genetic-based Simulated Annealing (CGSA) optimization scheme is introduced in Section 3 for IP-core mapping and topology selection. Section 4 demonstrates simulation results of validating our work. Finally, we summarize the related work in Section 5 before concluding the paper in Section 6.

2. Reliability estimation model

Silicon waveguide bend/crossings and Micro-Resonator (MR)-based photonic switching elements are extensively used in Optical Routers (ORs), and their cumulative crosstalk noise degrades the SNR, thus leading to a high bit error rate, which directly menaces the reliability of 3D ONoCs. In addition, different communication requirements among IP cores cause an unbalanced thermal characteristic at various locations of the 3D ONoC. Thus, our novel reliability model is divided into two parts: SNR model and thermal model, in order to measure crosstalk noise and thermal balancing, respectively.

2.1. SNR analysis

We define the SNR as the ratio of the optical signal power P_S over the crosstalk power P_C, which can be written as Eq. (1).

$$SNR = 10 \log\left(\frac{P_S}{P_C}\right) \tag{1}$$

Our SNR model mainly has two parts: intra-OR SNR and inter-OR SNR. More specifically, we first calculate the intra-OR SNR based on the structure of ORs, and then statistically analyze inter-OR SNR in the packet and network levels.

2.1.1. Intra-OR SNR

The internal structure of ORs is shown in Fig. 2, which is built from waveguide bends, waveguide crossings and two types of 1×2 switching elements including Parallel Element (PE) and Crossing Element (CE) [9].

As shown in the left part of Fig. 2: a waveguide bend incurs a bending loss L_b, and if P_{in} is the power of the input optical signal, the

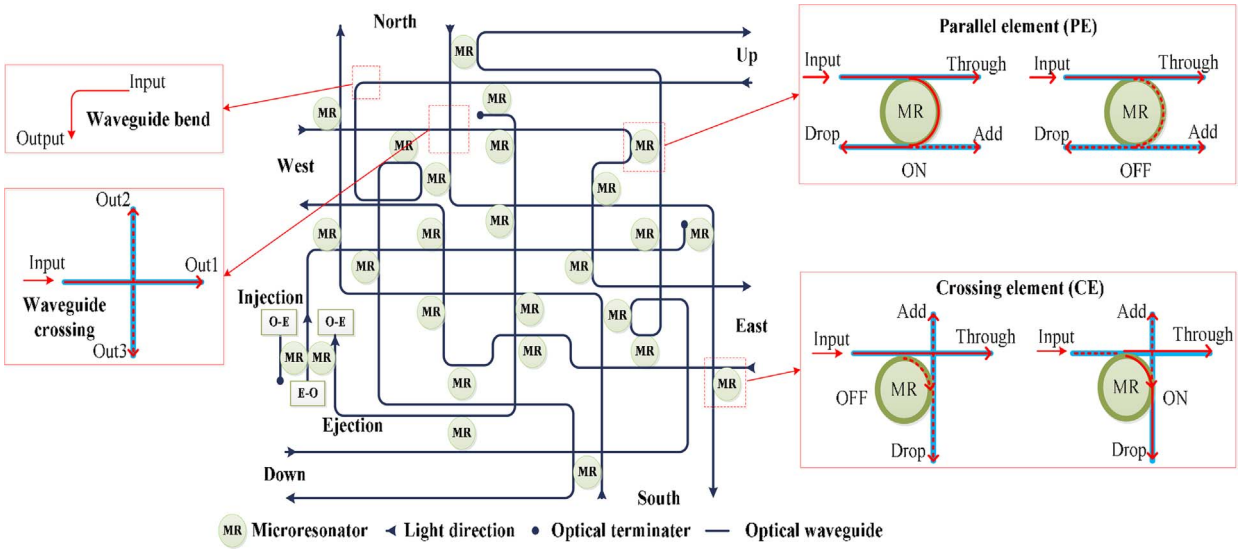

Fig. 2. Internal structure of optical routers.

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