INTEGRATION the VLSI journal 60 (2018) 13–24

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

Register Pre-Allocation based Folded Discrete Tchebichef Transformation Technique for Image Compression

M. Kiruba*, V. Sumathy

Electronics and Communication Engineering, Government College of Technology, Coimbatore 641013, Tamil Nadu, India

ARTICLE INFO

Keywords:
Discrete Cosine Transform (DCT)
Discrete Tchebichef Transform (DTT)
Floating Point Processing Element (FPPE)
Image Compression
Partial Cross Split Vedic Multiplier (PCSVM)
Register Pre-allocation Folded Architecture (RPFA)

ABSTRACT

Recently, the large size data, power and real-time processing abilities are major issues in Digital Signal Processing/multimedia applications which require an adaptable architecture. The tool used for computing data decorrelation in the image processing applications refers Discrete Tchebichef Transform (DTT) which offers better performance than the DCT due to its bitstream coding capabilities. This paper proposes a novel model of Discrete Tchebichef Transform (DTT) architecture with Register Pre-allocation based Folded Architecture (RPFA) for image compression. Through the cross-connection of folded architecture, the number of register usage is reduced. A Partial Cross Split Vedic Multiplier (PCSVM) method is introduced in the proposed DTT architecture. This multiplier design involves the cross function of the Vedic multiplier with the split pattern of multiplication binary stream. The optimal design of DTT architecture yields a minimum amount of FlipFlop (FF) counts, a latency and power consumption. The proposed PCSVM achieves higher Peak Signal to Noise Ratio (PSNR), better Structural Similarity Index (SSIM), lower delay, area, power consumption, Power-Delay Product (PDP), Mean Square Error (MSE) than the existing multiplier architectures. The proposed RPF-DTT architecture achieves a significant reduction in the resource consumption than the exact and approximate DTT architectures.

1. Introduction

Recently, the large size data, power and the real-time processing abilities are major issues in Digital Signal Processing/multimedia applications and the adaptable architecture is the immediate requirement to alleviate such issues. The performance of the entire system always depends on the top-level array interconnection and processing cell. The constructional issues of the top-level array and processing cell limit the throughput level adversely [1]. Hence, the extensible arithmetic processing elements are required to provide the guarantee to increase the throughput level. Based on the application requirements, the optimization and the prior knowledge are necessary during the design of processing elements such as registers, arithmetic units and control units. An orthogonal approximation of the Discrete Cosine Transform (DCT) is the major specification for the video and image processing applications. The good integer-based approximation of DCT coefficients plays the major role in the exact computation of transforms. The utilization of more number of registers for arithmetic operations and storage of results introduced the complexities in hardware design and huge power consumption. This paper focuses on the design of cross-connection of folded architecture to reduce the registers utilization in order to achieve less power consumption. High Efficiency Video Coding (HEVC) standard preceding the project called H.264/MPEG-4 AVC [2] specifies the definition of the semantic meaning of the syntax elements for the mapping of decoded pictures. The optimization of implementation process according to the application constraints and the prior knowledge regarding the implementation are the major requirements to meet the specifications of H.264/AVC. Discrete Cosine Transform (DCT) [3] and Just Noticeable Distortion (JND) [4] in H.264 have a major attention recently to adjust the quantization level to the threshold through the multiplication factor. The DCT also has the ability to support many video and image processing applications. An orthogonal approximation of 8-point DCT development in the research meet the specifications defined by the various image and video processing standards. The minimum complexity is the key characteristic in the combination of image compression with the quantization [5]. The good approximation of DCT coefficients plays the major role in the achievement of estimated results approached to the theoretical formulation. The integer-based approximations [6–8] act as an alternative approach for exact computation of the transforms. Real-time processing and the image transmission among the devices requires the suitable encoding algorithm with

* Correspondence to: Department of Electronics and Communication Engineering, Government College of Technology, Coimbatore, Tamil Nadu, India
E-mail address: kiruba.m1826@gmail.com (M. Kiruba).

http://dx.doi.org/10.1016/j.vlsi.2017.07.003
Received 9 September 2016; Received in revised form 6 June 2017; Accepted 7 July 2017
Available online 10 July 2017

minimum complexity level. Listless Set partitioning embedded blocK (LSK) and Set Partitioning Embedded bloCK (SPECK) are considered as the low-complexity image encoding algorithms and they are simple to implement. The encoding of each insignificant band as zero increases the size of zeros in earlier passes and this leads to high-bit plane operation. An improved LSK (ILSK) algorithm coupled with the Discrete Tchebichef Transform [9] achieves the desirable properties such as reduction in length of bit string, time and memory consumption effectively. The number of registers utilization for multiplication and the storage of results are more in such DTT. This paper focuses on the design of cross-connection of folded architecture to reduce the registers utilization in order to achieve less power consumption.

1.1. Motivation

Recently, DTT [10] has been used as a significant tool for image processing applications. The 8-point DTT outperforms the 8-point DCT in terms of average bit-length and high image quality [11]. The DTT-based architecture provides the better performance compared to DCT approach. Oliveira et al. [12] introduced a low-complexity approximation with multiplication-free transform for DTT. This differs from the traditional DTT transform by interchanging cross-connected weight value in 8-point Fast Fourier Transform (FFT) design. The final output is obtained in the encoded form to represent the compressed image. The direct implementation of DTT depends on the number of multiplications constantly performed which leads to more time consumption. Senapati et al. [13] provided the DTT implementation through constant multiplication of coefficients. They proposed the multiplier architecture that used the distributed based technique for high speed operation. The decoding operation enables reconstruction of the original image data. The proposed approximation ensures low-complexity and better performance according to meaningful image quality measures. Moreover, it consumed roughly one-third of the area and low power required by the exact DTT. But, the main drawbacks of this approximation architecture are increased latency and delay rate due to the more number of register usage. Hence, an improved DTT architecture with minimum delay rate is to be developed.

1.2. Our Proposed Work

A number of components such as adders and shifters used for the folding transformation structure are more [14] and hence the design strategy is modified with the register pre-allocation mechanism to reduce them. The total number of components involved in the existing architectures disrupt the overall performance of the image processing system with more delay rate, power dissipation, area consumption, etc. Moreover, the inclusion of more number of buffers and logical components also degrade the performance in the FPGA architecture. The brief study of background of 2-point DTT highlights the following major issues: The logical blocks included to perform the mathematical formulations are more in the folding transformation architecture, the meaningful image coordinates is the major requirement for the approximated low-complexity DTT architecture, more number of multipliers to perform the DTT process caused the hardware design complexities, area occupation and power consumption are more and hence the optimal components utilization still the major issue in DTT design.

To overcome these drawbacks, the number of components used in the FPGA architecture is to be minimized.

This paper proposes a new model of DTT architecture with RPFA and PCSVM. RPFA is used for reducing the number of register usage through the cross-connection of folded architecture. The FPPE architecture and optimal size of multiplier design reduced the number of multiplier usage and number of adders in the complex image transformation process. Since DTT performs image transformation with the help of FFT and Inverse FFT (IFFT) process, it achieves the minimum amount of pixel loss in an image. The optimal design yields the minimum amount of FF counts and latency. These optimal delay elements will improve the throughput rate of overall design. The major contributions of proposed PCSVM with RPFA are listed as follows:

The major contribution of proposed work is to reduce the size of the DTT architecture in image compression applications. The folded transform architecture includes the floating point Arithmetic and Logical Unit (ALU) with the adder blocks to perform the transformation. The optimal allocation of registers prior to the transformation process reduces the time delay and latency. Initially, the code streams corresponding to the input image are generated from the pixel matrix. The matrix form of the image representation splits up into the several major blocks for the effective computation. The code stream and the split-up form are used to select the points necessary to describe the target region. Then, the data transfer in and out from the blocks are maintained in the state table form which is the necessary stage in the folder architecture. On the basis of state declaration from the table, the registers required for the manipulation operations are pre-allotted to reduce the delay. The operation of the folded architecture (with ALU and adders) is controlled with the help of state machine values. The responsible variable corresponding to the controller status is loaded into the output registers. The output values for each state are accumulated in the output registers which are regarded as the DTT output if the simulation completed.

The comparison result of the proposed work with existing architecture in terms of both design parameters and application parameters describes the efficiency of the RPF-DTT and PCSVM. Our proposed architecture is compared by using the application parameters such as delay, area, power and PDP and design parameters such as Number of FFs, Look Up Tables (LUTs), Clock frequency, Latency, Delay rate and Throughput. The proposed PCSVM achieves higher PSNR, better SSIM, lower delay, area, power consumption, PDP and MSE than the existing multiplier architectures. The proposed RPF-DTT architecture achieves reduction in the resource consumption than the exact and approximate DTT architectures.

1.3. Objectives of our work

The main objectives of our proposed work are listed as follows

The Partial Cross Split Vedic Multiplier (PCSVM) included in the proposed model considers the cross function with split pattern multiplication of binary stream to reduce the total number of adders and shifters. The pipelined architecture with the pre-register allocation mechanism reduces the usage of the multipliers and registers effectively. Due to this reduction, the delay and power are reduced. The re-utilization of logical components under the register arrangement cycles reduces the delay rate (ns). The folding and crossing of data lines with the Butterfly (BF) block reduces the number of multiplication stages. The BF block has the ability to transform the complex input points to the complex output points. The transformation process needs a complex multiplication that requires the new architecture called Floating Point Processing Element (FPPE).

1.4. Organization

The remaining sections of the paper are organized as follows: Section II presents a brief overview of the existing DTT architectures used in the image processing applications. Section III describes the DTT including the existing DTT and proposed architecture including FPPE design, RPFA and PCSVM. Section IV illustrates the performance analysis results including the design summary of the proposed PCSVM and RPF-DTT architecture. Section V involves the comparative analysis of the proposed PCSVM and RPF-DTT architecture with the existing multiplier architectures and DTT architectures. Section VI gives the conclusion and future implementation of the proposed work.