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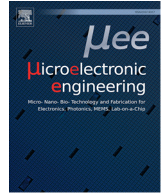

Technical note

Fabrication of a nano-scaled tri-gate field effect transistor using the step-down patterning and dummy gate processes

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ABSTRACT

The process sequence and device performances of the three-dimensional tri-gate field effect transistor (TGFET) were reported, where a fin-shaped Si channel with a 20 nm channel width and an 80 nm fin height was fabricated using the conventional *i*-line stepper, assisted by the double hard mask step-down (DHMSD) lithography process. The channel length was 150 nm. An atomic-layer-deposited Al_2O_3 film with an equivalent oxide thickness of 1.9 nm and a TiN layer grown through another atomic layer deposition process were adopted as the high-k and metal gate, respectively, using the dummy gate process. The device performance was compared with that of the planar FET simultaneously fabricated on the same Si wafer. The ion implantation and Ni-silicide processes were also optimized for this process sequence. Both n- and p-type devices were fabricated. The TGFET showed a high on/off current ratio of ~10^6, a low subthreshold swing of 105 mV/dec for the n-type device, and a small drain-induced barrier lowering of 30 mV for the n-type device, which were remarkably improved device performances compared with the planar FET device. These improvements were due to the improvement of the electrostatic control of the fin-shaped channel by the tri-gates, which coincides with the theoretical expectation and previous experiment results. Nevertheless, the p-type devices showed inferior performances compared with the n-type devices due to the excessive dopant diffusion from the source and drain regions into the channel.

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1. Introduction

The advantages of metal oxide semiconductor field effect transistor (MOSFET) scaling are quite substantial due to the increase in the functionality per unit chip area and its performance, cost reduction per functionality, and device switching power. MOSFET scaling in logic devices has been following the well-known Moore's law, although the law itself has been modified several times during past several decades, and it was recently announced that the semiconductor industry will no longer follow the law [1]. After the setting up of the fundamental configuration of the complementary MOSFET (CMOSFET) in the 1960s, it was not changed in the next ~40 years, but the adoption of the high-k/metal gate (HKMG) process in 2007 was a remarkable technical breakthrough in the field. Another radical change in the MOSFET structure occurred in 2014, when the tri-gate FET (TGFET) or fin-shaped FET (finFET) started to be mass-produced. While the concept of adopting such three-dimensional FET structure had been suggested by Hu et al. [2] for silicon-on-insulator (SOI) devices in the 1990s, its adoption in mass production has been hampered by the high cost of the SOI wafers and other technical issues. The later suggestion of Lee et al. [3,4] on the use of the bulk Si finFET marked another critical improvement in the CMOSFET circuit, making the mobile information technology keep its growing pace.

The fundamental idea of TGFET (or finFET) is to increase the channel width (W) for the given channel length (L) without increasing the Si surface area consumption, and the tri-gate configuration is a highly feasible structure for achieving this goal [5,6]. This goal can be accomplished by increasing the fin height (H_{fin}) for the given fin width (W_{fin}). Fabricating the fin-shaped Si channel, however, requires highly elaborate process optimization, and among the methods for such, the patterning of the tiny fin with a W_{fin} lower than ~20 nm is critically important to acquire the expected merit on the device operation due to the improved electrostatics compared with the planar-geometry devices. The currently available most advanced lithography apparatus adopts ArF laser with a 193 nm wavelength (λ), which is too long for patterning such small features. Therefore, the industry has developed numerous resolution enhancement techniques, including the immersion lithography process and the double or quadruple patterning techniques, which allowed the state-of-the-art level lithography to decrease to ~10 nm. While these are astonishing achievements in the industry, they are usually not feasibly available in the academe mainly due to the very high cost of the equipment and operation. Therefore, a feasible option for the academe is the electron-beam lithography, but optical lithography is still preferred method if it can provide the necessary feature size. If

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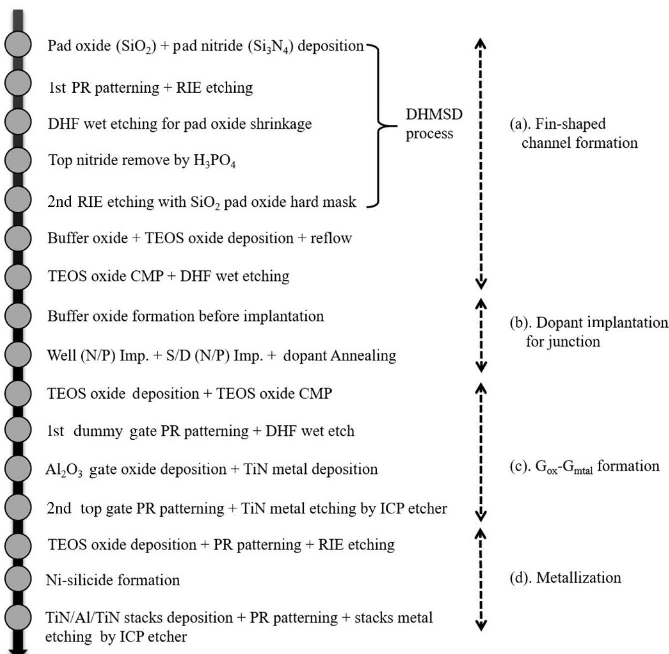
this process can be successfully set up in the academe, it will further accelerate the development of this critically important area.

In this work, therefore, the authors developed a full process sequence to fabricate a tri-gate CMOSFET with a 20 nm W_{fin} using an *i*-line stepper (NSR-2005i10C, Nikon, $\lambda = 365$ nm). Planar-geometry CMOSFETs were concurrently fabricated on the same wafers, which allow the precise assessment of the performances of two device types: planar and TGFETs. As the affordable resolution of the stepper is far lower than the intended pattern size (W_{fin}), a specific line width decreasing technique was developed, which is called "double hard mask step-down (DHMSD) patterning process," using SiO_2/Si_3N_4 double hard mask layers. As the channel has a three-dimensional structure, conformal film growth techniques are required for the high-k gate insulator and gate metal. Therefore, atomic-layer-deposited Al_2O_3 and TiN were used as the gate insulator and metal gate, respectively, where the dummy gate process was adopted to minimize the adverse effects related with the gate etching process. The fabricated CMOSFETs with a tri-gate structure showed a far superior performance than the planar devices, as expected, but the p-type devices showed characteristics revealing the limitation of the adopted process, especially the dopant activation step, which requires further process optimization.

2. Device fabrication

The fabrication of the TGFET process started with 6-inch p-type bulk silicon wafer. All the processes were performed in a clean room, and the class was 100. Table 1 shows the overall process sequences. The process flows are divided into four parts: channel formation (part (a)), implantation (part (b)), gate oxide (G_{ox})-gate metal (G_{metal}) formation (part (c)), and metallization (part (d)). The fin-shaped channel formation part consists of the DHMSD process for achieving a small W_{fin} (20 nm) and the gap fill process for the isolation between the channel and the substrate. The dopant implantation part had four steps of doping for the n-channel, p-channel, n-type source/drain (n-S/D), and p-type source/drain (p-S/D). The G_{ox}-G_{metal} formation part consists of the dummy gate process on a high-fin-height structure to minimize channel damage by the etching processes. Lastly, the metallization part has Ni-silicide for the Ohmic contact formation and Al metal formation for

Table 1
Fabrication flowchart of the nano-scale TGFET fabricated through the double hard mask step-down patterning (DHMSD) and dummy gate patterning processes.



the contact pad open area. The entire process scheme was based on the gate-last [7] integration scheme, which is characterized by the deposition of the HKMG stack after the high temperature dopant activation annealing. Each process will be described with a detailed explanation in the following subsections.

2.1. Double hard mask step-down patterning process

The p-type Si wafer was cleaned through sequential standard cleaning-1 (SC-1, $NH_4OH:H_2O_2:H_2O = 1:1:5$, 60 °C) and standard cleaning-2 (SC-2, $HCl:H_2O_2:H_2O = 1:1:7$, 80 °C) for particle removal. SC-1 cleaning is effective for organic particle removal and surface conditioning, and SC-2 is efficient for metallic particle removal [8]. After cleaning, DHMSD patterning process was started with the hard-mask film stacks, as shown in Fig. 1. The 50-nm-thick thermal SiO_2 layer grown through dry oxidation and the 30-nm-thick Si_3N_4 layer grown through low-pressure chemical vapor deposition (LPCVD) were sequentially stacked on the top of the cleaned Si wafer. The LPCVD Si_3N_4 film was grown at 700 °C using dichlorosilane (DCS, SiH_2Cl_2) and NH_3 gas ambient. The SiO_2-Si_3N_4 stacked films would play a role in the hard-mask etching for the following first lithography patterning. From those stacks, initial lithography by the *i*-line stepper was started using an 800-nm-thick photoresist (PR) film. The first lithographic exposure of the PR film and the following reactive ion etching (RIE) of the hard mask (Si_3N_4-SiO_2 stacks) could define the 400 nm width pattern of the SiO_2-Si_3N_4 stacks without any etching of the Si substrate, as shown by step 3 in Fig. 1. RIE was performed with CHF_3, CF_4-Ar mixed etching gas, and 600 W plasma power. Then, the width of the SiO_2 layer was decreased to the desired value (20 nm) through wet etching with diluted HF (DHF, HF: $H_2O = 1: 7$) etchant for 100 s while the top Si_3N_4 layer played the role of the protection layer for the SiO_2 hard mask being etched from the top portion. The established sideways wet etching process showed a 1.4 nm/s etch rate per side, meaning that the 20 nm width of the SiO_2 layer must be remained after the 100-sec-long etching (step 4 in Fig. 1). After this step, the cross-section of the sample was examined via transmission electron microscopy (TEM), as shown in Fig. 1(b), where the SiO_2 hard mask with an 18 nm width at the middle portion was well formed under the 400-nm-wide Si_3N_4 mask layer. To remove only Si_3N_4, H_3PO_4 stripping was carried out at 180 °C, which is effective for removing only the Si_3N_4 layer, without attacking the SiO_2 mask (step 5 in Fig. 1). After removing Si_3N_4, only the shrunk SiO_2 pattern became exposed, which worked as the hard mask for the second RIE step for Si fin channel formation. This second RIE step was performed with HBr and O_2 gas and 900 W main power. The H_{fin} can be varied from 80 to 250 nm by varying the second RIE time from 20 to 60 s. This RIE step also included the etching step for shallow trench isolation (STI). Fig. 1(c) shows the TEM cross-section image of the fin-shaped Si channel formed through the process sequence mentioned above, where the 18–19 nm W_{fin} at the middle portion was clearly defined.

2.2. Gap-fill process

For STI formation, gap filling was conducted as described in Fig. 2. After finishing the DHMSD patterning process, a 10-nm-thick SiO_2 thermal buffer oxide layer was grown on the fin Si channel through dry oxidation, and the entire wafer was deposited by another LPCVD SiO_2 film using tetraethyl orthosilicate (TEOS) and O_3 as the reaction gases (TEOS oxide) (step 2 in Fig. 2). The 650-nm-thick TEOS oxide film was used as the STI gap fill material [9], and the CVD TEOS oxide film was reflow-annealed at 950 °C for 30 min. Chemical mechanical polishing (CMP) of the TEOS oxide film was subsequently carried out for planarization, which is important to achieve a uniform leveling down of the STI gap fill oxide when the next DHF wet etching process is applied for fin-shaped channel exposure (step 4 in Fig. 2). At this time, the 10-nm-thick SiO_2 buffer oxide played a critical role in the uniform wet etching of the STI gap fill oxide. If this buffer oxide is not adopted, the wet

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