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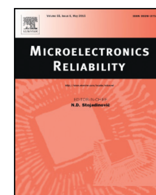

Avalanche robustness of SiC Schottky diode

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ABSTRACT

Reliability is one of the key issues for the application of Silicon carbide (SiC) diode in high power conversion systems. For instance, in high voltage direct current (HVDC) converters, the devices can be submitted to high voltage transients which yield to avalanche. This paper presents the experimental evaluation of SiC diodes submitted to avalanche, and shows that the energy dissipation in the device can increase quickly and will not be uniformly distributed across the surface of the device. It has been observed that failure occurs at a fairly low energy level (<0.3 J/cm^2), on the edge of the die, where the electrical field intensity is the greatest. The failure results in the collapse of the voltage across the diode (short-circuit failure mode). If a large current is maintained through the diode after its failure, then the damage site is enlarged, masking the initial failure spot, and eventually resulting in a destruction of the device and an open circuit.

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1. Introduction

Silicon carbide Schottky diodes are attractive devices to replace silicon rectifiers in several applications as they offer many superior properties (high voltage capability, very low switching losses and little stored charge). In some applications such as HVDC converters, many diodes are used in series to increase the blocking voltage. Generally, homogeneous voltage distribution has to be forced: in blocking-state by using parallel resistors; during commutation using parallel RC [1]. Nevertheless, in some cases, the voltage may not divide equally across the series string of diodes. A transient of sufficient amplitude will drive the voltage across one or more diodes into the breakdown region.

In general, SiC Schottky diodes suffer from their very limited avalanche breakdown stability due to the avalanche current filamentation at the Schottky interface or the edge termination [2]. The avalanche test is an essential reliability standard test for high-power devices as this phenomenon may happen in every switching converter or inverter during transient operating modes.

The test allows to obtain data about the capability of SiC Schottky diodes under avalanche operation. They provide key information about how to design a Schottky diode, which can limit the effects of avalanche on the devices and provide protection for the application.

Destructive failure under avalanche operation has been studied extensively for many power devices such as MOSFETs and IGBTs [3,4] but more recent devices such as SiC Schottky diodes have not yet been investigated as much. Zhang et al. have presented a failure mechanism analysis for Schottky diode [5]. It has been reported that the avalanche breakdown is considered as the main catastrophic failure mechanism of Schottky diodes. As in any semiconductor or metal/semiconductor junction, under excessive electric field, the thermally generated electrons and holes get enough kinetic energy to knock on atoms, which then generate more electron-hole pairs within the diode. This results in high reverse current generated within the device. As a consequence, the power dissipation increases in a localized spot which then destroys the device thermally [6].

This paper proposes a thorough experimental test of the performance of commercially available SiC Schottky diode under avalanche conditions. The remainder of this study is organized as follows: the avalanche tester and the operating principle is presented in Section 2. Section 3 describes the results concerning the reliability of tested SiC Schottky diode under avalanche conditions. Section 4 shows some discussions about the failure mechanisms that limit the device reliability. Finally conclusions are given in Section 5.

2. Experimental setup

2.1. Description of the bench

The circuit diagram of the experimental setup is shown in Fig. 1. It includes the following parts: a high voltage power supply (0…3 kV DC) charges up a film capacitor C (1250 μF, 3 kV). The stored energy is used to produce the avalanche conditions.

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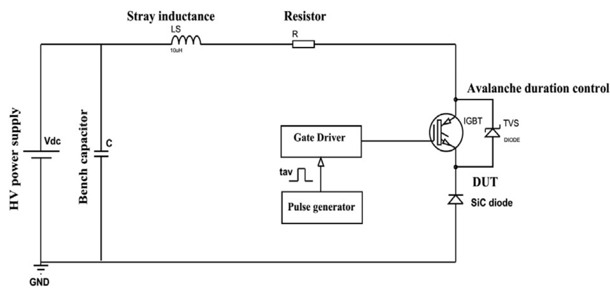

Fig. 1. Schematic of avalanche test circuit for SiC Schottky diode.

An IGBT controls the duration of the high voltage pulse applied to the device under test (DUT) and a resistor is used to set the current during the avalanche [7]. The control IGBT can be switched off immediately after the failure of the DUT to avoid its explosion. For safety reasons, the circuit is placed in a closed system, visible in Fig. 2, which includes the high voltage power supply, the capacitors, the test zone, and a control panel (other features are included but not used in this article, such as over-current detection, active current limitation, etc.). An interlocking mechanism, connected to high voltage contactors, prevents any accidental contact with high voltage. The implementation of these safety systems required in a fairly long cabling between the capacitors and the test zone, resulting in a total stray inductance estimated at 10 μH.

This test circuit is fairly different from the commonly used (and described in a JEDEC standard [8]) "Unclampled Inductive Switching" (UIS). Here, the energy tank is a capacitor (instead of an inductor in the case of UIS). Using a capacitor is less practical, as it requires a high voltage power supply and an accurate control of the voltage. However, the same capacitor bank can also be used for short circuit tests (not described in this article). This makes the test bench more versatile, which is why we chose this solution.

The main specifications of the experimental setup are summarized in the following table: (See Table 1).

2.2. Test protocol

In this paper, we investigate a 1200 V SiC Diode (C4D20120A from Wolfspeed). The devices under test are single chip in TO220 package, the rated characteristics of this devices are shown in Table 2.

Table 1
The main specification of the experimental setup.

Characteristic	Value
Maximum voltage	3 kV
Maximum current	500 A
R resistor	10 or 50 Ω
C capacitor	1250 μF
Stray inductance	10 μH
Avalanche duration control	HITACHI MBM500E33E2 3.3 kV, 500 A

Table 2
Rated characteristics of tested SiC Schottky diode.

	Power device	VRRM (V)	IF (A)	Die size (mm^2)
DUT	SiC diode	1200	20	3.1 ∗ 3.1

Avalanche tests are performed with a current limiting resistor of either 10 or 50 Ω. In each configuration, an avalanche duration is fixed (a different one for each device tested). Then, the DC voltage is gradually increased from a low value (where the device is able to sustain the avalanche conditions) up to the failure. Before failure, the device can survive many voltage pulses. Once failed, the device is no longer able to sustain the full DC voltage. The energy leading to the device failure is determined by measuring the reverse current and voltage using respectively a Pearson current monitor model 4997 and a high voltage probe (PHV 662-L) from PMK. This energy is called the critical energy *EC*, which is an essential feature of robustness to SiC Schottky diode. It can be calculated as the time integral of the product of the reverse voltage V_d and the reverse current I_d (see Fig. 3).

$$E_c = \int_{t_1}^{t_2} V_d(t) \cdot I_d(t) dt \tag{1}$$

Fig. 3 shows the typical set of waveforms obtained under avalanche operation, when a device fails: V_{GE} is the gate signal applied to the control IGBT (red); I_d is the reverse current in the DUT (green); V_d is the reverse voltage measured across the DUT (blue) and *E* refers to the energy dissipation of the device (gold). As it can be seen, V_d is initially equal to $V_i \approx 0$ when the IGBT is off. Once the pulse is applied through the IGBT ($t_1 \leq t \leq t_3$), and if the DC voltage exceeds the breakdown voltage ($V_{BR} < V_{DC}$) of the diode, some current flows through the diode. At this

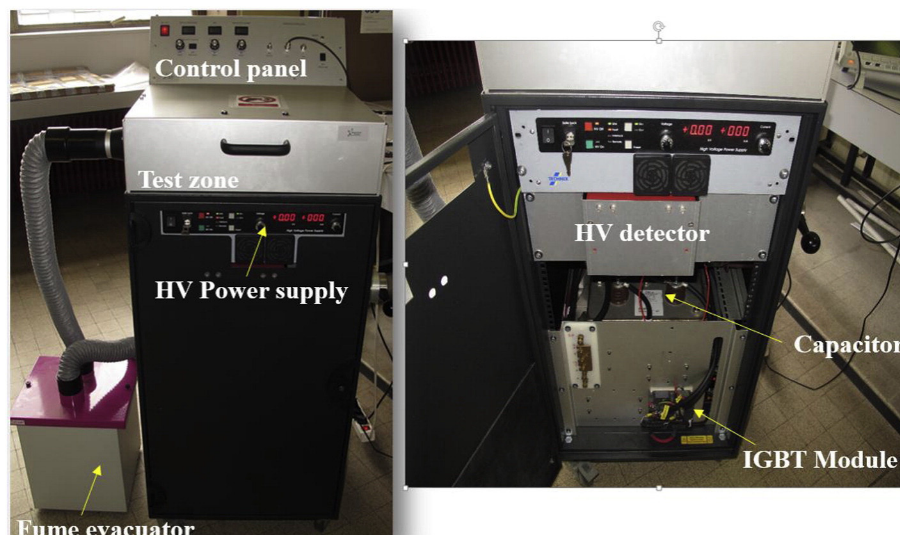

Fig. 2. Picture of the experimental setup using the power circuit in Fig. 1.

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