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Review

Modulation techniques applied to medium voltage modular multilevel converters for renewable energy integration: A review

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ABSTRACT

Modular multilevel converters (MMC) inherent features are gaining more attention for dc voltage transmission systems. One of the main research paths regarding the converter performance deals with its voltage modulation. Specifically, for medium voltage applications with relatively small number of submodules, the voltage modulation techniques impact on the MMC performance needs to be studied.

This work provides an extensive review of the carrier-based pulse with modulation (CB-PWM) techniques proposed to be applied on previous multilevel inverter versions. The CB-PWM methods were adapted to be compatible with an additional cell ranking and selection algorithm to ensure equal energy distribution on the arm cells. The state-of-the-art of zero sequence signals (ZSS) applied on three-phase inverters is also reviewed. The alliance between the ZSS with the CB-PWM, as well as the nearest level modulation (NLM), has an important impact on the MMC harmonic content, efficiency and voltage ripple of its cells capacitors. A 15 MW 28-cell-based MMC is used to investigate each particular combination between the modulation method and the common mode ZSS.

Contents

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1. Introduction

The modular multilevel converter (MMC) is a reasonably young inverter technology with a promising future in medium voltage DC (MVdc) systems, such as large wind turbines in the DC collection grids, large PV integration, large marine current and wave energy integration [1–4]. Modularity, redundancy and high quality voltage waveforms make the MMC a viable solution for dc transmission applications [5–8]. However, the arms voltage management evokes several concerns on its performance.

Over time, several modulation techniques have been proposed to compile the required ac voltage at the output of the multilevel-based voltage source converters [8–15]. Most of the proposals were carrier-based PWM (CB-PWM) and depending on the nature of the corresponding carrier, different pulse patterns are applied to the converter's switches. Hence, different voltage profiles and performances were conceived for the VSC's.

This work presents a review of the CB-PWM techniques proposed for the previous multilevel VSC generations. Then, the relating strategies were considered to shape the voltage generated on the MMC's arms in combination with an additional capacitor's energy balancing algorithm. Additionally, the performance of the presented modulation strategies was complemented with the impact analysis of the zero sequence signals (ZSS) injection into the MMC arms modulation. A medium voltage-based MMC model with 15 MW/28 submodules is embraced to analyze the impact of several arm voltage modulation strategies on the converter performance, namely, on its efficiency, capacitors ripple and quality of its waveforms.

This paper is organized as follows: Section 2 presents and discusses several modulation strategies and zero sequence signals proposed in the literature that can be used to improve the operation of the inverters. The methodology followed to assess the performance of the MMC is discussed in Section 3. The impact of the modulation strategies on the converter performance is then argued in Section 4. The final remarks are presented in Section 5.

2. Multilevel modulation techniques

Several modulation strategies have been introduced to drive multilevel converters, namely for Neutral Point Clamped (NPC) [16], Flying Capacitor (FC) [17] and Cascaded H-Bridge (CHB) [18–22] and, more recently, modular multilevel converters [23,24]. The first three VSC structures require proper PWM-controlled strategies to balance the energy storage of their dc-bus capacitors, without the use of additional hardware [25,26]. Once the control scheme of these converters determines the require voltage target for their output u_j^*, it is normalized in accordance with the maximum voltage amplitude achievable at the VSC's output, particularly, the dc-bus voltage U_{dc} as:

$$m_j^* = \frac{u_j^*}{U_{dc}} \tag{1}$$

The correspondent modulation index m_j^* of a M-level converter is then compared with (M-1) carriers, resulting then in 2(M-1) logical signals to drive the correspondent switches of each converter leg. The intrinsic features of each CB-PWM techniques and their redundant voltage vectors are responsible for balancing the dc capacitors voltages [21].

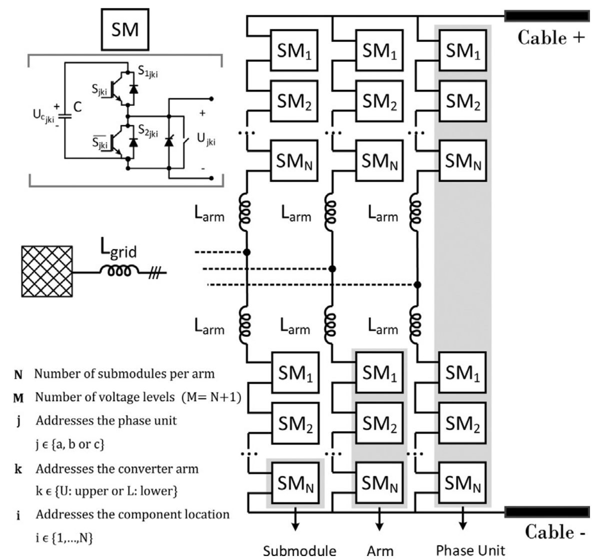

Fig. 1. Three-phase circuit of the modular multilevel converter.

In terms of the MMC, as presented in Fig. 1, the energy is no longer stored on its dc side bus but instead in the capacitors placed inside the submodules (SM). Due to the converter nature, the grid currents flow directly on the SM's capacitors and this situation establishes a great voltage ripple variation. As a result, the energy stored in the capacitors tends to diverge over the time, which emerges the need for balancing their energy to achieve a proper converter operation [27,28]. This goal is addressed by selecting the proper redundant voltage vectors on the MMC arms, but this stage is done by means of a selective control of the cells.

So, if in the NPC, FC and CHB solutions, the CB-PWM techniques are used to shape their output voltages and to balance the energy storage of their floating capacitors [29], regarding the MMC this is done in more stages. The consequent stage of defining the required voltage to be synthesized across the converter arms u_{jk}^* is the determination of the arm modulation index target m_{jk}^* (2). Later on, the suitable number of on-state cells are determined by means of the multilevel modulation schemes. Thereupon, the cell selection methods are required to ensure controlled energy distribution between the capacitors within the same stack [27,30]. The flexibility allowed by sorting and selecting the MMC capacitor's to be inserted, besides the knowledge of their individual voltages, also permits a decision on which capacitors are inserted in the chain depending on the SM's semiconductors temperatures [31].

$$m_{jk}^* = \frac{u_{jk}^*}{U_{jk}^{\Sigma}} \tag{2}$$

The arm voltage modulation stages applied in the MMC are depicted in Fig. 2. The stage 1 is defined by the admittance of zero sequence signals injection into the converter modulation, which is discussed in Section 2.1. The second stage consists in defining the suitable number of capacitors that should be inserted on the converter arms. Several techniques can be embraced and further analysis is presented in Section 2.2. In Section 2.3 the selective control scheme of the MMC cells is explained.