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Image Processing of Composite Video with FPGA Programmable Logic

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Abstract: Described project presents a hardware solution of Image Processing Unit based on a Spartan-6 FPGA programmable logic. The unit consists of a digitizing videoconverter module (Kasik, 2011), NEXYS 3 board with FPGA (Digilent, 2013) and a color TFT touch screen display (Digilent, 2011). As the video source for the videoconverter serves a composite video output from the Canon MV530i camcorder (Canon-europe, 2002). The output of the video converter is in parallel ITU-BT.656 data format. The video processing unit implements several functions which include conversion to RGB colors, Grayscale, Black and White, Sepia and Edge Detector. The complete FPGA logic is designed in VHDL and many modules are in the form of parameterized IP cores. The resulting video is demonstrated on the TFT display, which also serves for controlling the implemented functions. The project was created for educational purposes as demonstration of video signal processing on FPGA.

Keywords: Image Processing, ITU-R BT.656, FPGA, Programmable Logic, Threshold, Edge Detect.

1. INTRODUCTION

Although currently most cameras on the market are with a digital output, eg. as a webcams, cameras in mobile phones, tablets, etc., among many devices are still used composite video output. In such cases, there is not common any additional image processing, for example, detection of objects in the image. For such a procedure the input image usually should be converted into a form that search algorithms are most effective. These operations belong to the so called image pre-processing. Pre-processing typically involves blurring, brightness correction, resolution adjustment, applying various filters, convert to grayscale, convert to binary image and other operations. Some operations reduce redundant data and accelerate the pre-processing, while others adjust areas of interest for further processing. Most tasks in which the image processed are limited in time and effort is therefore these tasks as much faster. Use of programmable logic offers the possibility to relieve normal PC work and take some part of the process.

The design implemented in this work demonstrates image processing examples in programmable logic. FPGAs offer relatively large parallel processing capabilities. For this reason, it is not necessary to require such a high clock frequency of the digital logic, as in the case of conventional computer. Yet FPGAs with significantly lower frequency can be many times more powerful than commonly used computer. The signal source used in the project is implemented with a commercially available camcorder. The processed signal is fed and subsequently rendered to the screen. In practical use, it is possible to change the source of input data, eg. using image data from the CCD sensor with other digital interface. The project contains a few selected blocks for image processing, which can usually be used for processing of still images or moving video.

2. PROGRAMMABLE LOGIC FOR IMAGE PROCESSING

For the task of image processing were first selected a few basic functions that are commonly used in graphic programs on PC and sometimes in features of commercial electronics.

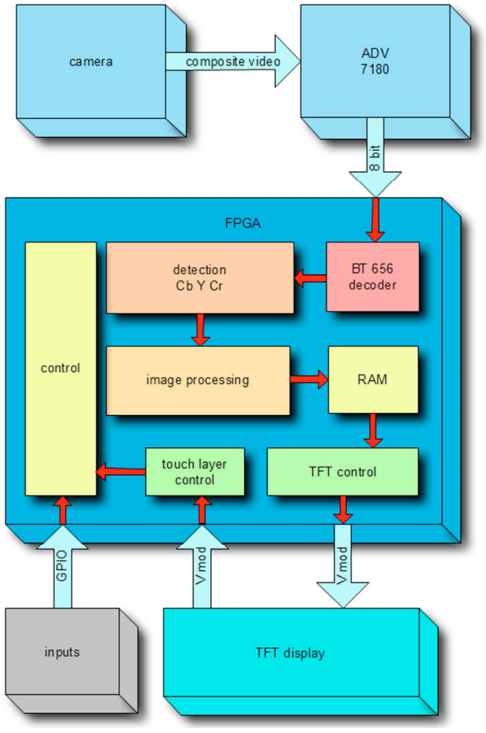

Fig. 1. Block diagram of the project.

These include conversion to RGB colors, Grayscale, Black and White, Sepia and Edge Detector. The hardware for implementation was chosen Xilinx's Nexys 3 Development Kit equipped with Spartan 6 FPGA, which meets common

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demands on computing power and flexibility. The kit contains useful peripherals such as VGA, seven-segment display, LEDs, switches and buttons. In addition to conventional peripherals it's equipped with a Digilent VHDCI (or Vmod hereafter) connector, which is used to connect the TFT touch screen display in the project. All created blocks are designed as IP cores in VHDL, which can be easily instantiated in other projects. Nevertheless, the project is designed for a Xilinx Spartan-6 FPGA family, all IP cores can be smoothly applied for any other programmable logic architecture. Individual functional blocks in the project are designed as separate VHDL modules and digital logic was created with respect to synchronous clocking when possible. However, due to several asynchronous processes used in the design it contains four different clock signals:

Table 1. Clock signals in the design

Clock signal	Frequency [MHz]	Description
clk	100	Board clock input
clk_vp	27	AD7873 clock reference
clk_tft	9	TFT display clock (positive)
clk_tft_180	9	TFT display clock (negative)

3. SOURCE OF THE VIDEO SIGNAL

As the video source is used a Canon MV530 camcorder (Fig. 2) in the project, which is also equipped with an output for composite video format CCIR PAL. This camera can of course be replaced by any other source of corresponding analog video signal. Composite video is then digitized in a digitizer block with an ADV7180 circuit.

Fig. 2. Canon MV530 camcorder.

The ADV7180 circuit contains three analog inputs equipped with anti-aliasing filters. Sampling of video inputs is carried out by an 86 MHz clock generated by on-chip PLL. Then a teletext data, luminance (luma) and chrominance (chroma) components are separated from the digitized videosignal. Finally, the data are written to the output in accordance with the ITU BT.656 standard. The whole circuit can be controlled using an I^2C bus. The module includes three RCA connectors for analog signals and twenty-pin ribbon cable connector to attach a parallel data bus, I2C communication, power supply and other control signals.

4. COLOR TOUCH SCREEN DISPLAY

For image viewing and control is used the Digilent's VmodTFT (Digilent, 2011) color display with 480x272 pixels resultion and 24-bit color depth. The connection to the development kit is provided via a 2x34 pin VHDCI connector.

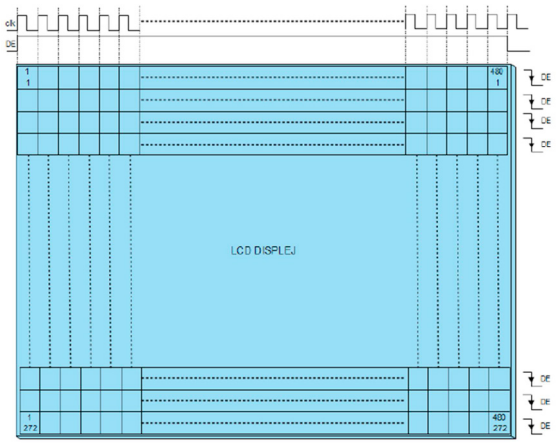

Fig. 3. Matrix display with control signals.

Pixel clock of the display can be in the range 7-12 MHz and must meet the time parameters specified in (Digilent, 2011).

4.1 Touch screen layer

The upper side of the display contains a touchscreen layer sensing compression by changing the resistance. It contains two conductive transparent layers with a thin gap between them. Each layer has a well-defined resistance see Tab. 2. On the opposite side of each layer are positioned electrodes.

Table 2. Touch screen layer resistance

Axis	Min. resistance [Ω]	Max. resistance [Ω]
X	300	1500
Y	100	900

When pressing the layers the connection between electrodes occurs. By measuring the voltage on the electrodes the touch coordinates can be calculated according to equations (4.1), (4.2).

$$x = \frac{V_x - 96_h}{F6E_h - 96_h} \cdot 480 \qquad (4.1)$$

$$y = \frac{V_y - 12C_h}{ED6_h - 12C_h} \cdot 272 \qquad (4.2)$$

wherein Vx and Vy are the measured voltages. The coefficients referred to in phrases are limiting resistor values for each of the corners of the screen, as shown in the Table 3.

Table 3. 12-bit coefficients for the boundary points of the touch layer

Corner	X coefficient	Y coefficient
Upper left	096h	12Ch
Upper right	F6Eh	12Ch
Bottom left	096h	ED8h
Bottom right	F6Eh	ED8h

As a circuit for controlling the touch layer serves AD 7873 that determines which electrodes will be at that time