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Fixed structure compensator design using a constrained hybrid evolutionary optimization approach

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ABSTRACT

This paper presents an efficient technique for designing a fixed order compensator for compensating current mode control architecture of DC – DC converters. The compensator design is formulated as an optimization problem, which seeks to attain a set of frequency domain specifications. The highly nonlinear nature of the optimization problem demands the use of an initial parameterization independent global search technique. In this regard, the optimization problem is solved using a hybrid evolutionary optimization approach, because of its simple structure, faster execution time and greater probability in achieving the global solution. The proposed algorithm involves the combination of a population search based optimization approach *i.e.* Particle Swarm Optimization (PSO) and local search based method. The op-amp dynamics have been incorporated during the design process. Considering the limitations of fixed structure compensator in achieving loop bandwidth higher than a certain threshold, the proposed approach also determines the op-amp bandwidth, which would be able to achieve the same. The effectiveness of the proposed approach in meeting the desired frequency domain specifications is experimentally tested on a peak current mode control dc – dc buck converter.

1. Introduction

Closed loop control of DC – DC converters are used to regulate the output voltage by changing the gate driven input to the switches. Typically, a Pulse Width Modulation (PWM) technique is used to generate the controlling signal. Under PWM control, a switching regulator may operate either in Voltage Mode Control (VMC) or in Current Mode Control (CMC). The fundamental difference between VMC and CMC is in the choice of the signal for PWM modulation. In VMC, a fixed frequency external ramp is compared with the output of the compensator to generate the duty cycle. Whereas, in CMC, cascade control architecture is used, where in the inner loop the sensed inductor current is compared with the control signal generated by the outer loop to generate the PWM signal. CMC is considered to be superior to VMC due to the fast inner current loop and is therefore widely used in high-performance power supply applications. Further advantages of CMC include current sharing, inherent current limit and lower order compensator [1].

For a power converter circuit, the compensator design process involves satisfaction of the following frequency domain criteria for the loop gain frequency response, which generally relates to the various time domain specifications.

- High Bandwidth (BW) for the loop, resulting in a faster response when subjected to load and line disturbances.
- Adequate Phase Margin (PM) (typically greater the 40°) to obtain low settling time and less overshoot.
- High Gain Margin (GM) (typically > 20 dB) for low sensitivity to high frequency noise.
- High low frequency gain (greater than 70 dB) for small steady state error.

The conventional approach of compensator design for industrial applications involves the use of fixed and low order compensators, generally referred to as Type-I, Type-II and Type-III compensators [2]. Type-II compensators are generally preferred for PCMC applications. The widely used K-factor method [3], directly calculates the compensator parameters based on the BW and PM specifications. Since in K-factor method, the parameters are represented mathematically as a function of the specifications, quite often the resulting solutions (parameters) are negative. Also, the op-amp non-idealities are not taken into account in the design

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Nomenclature

v_c	instantaneous capacitor voltage
i_l	instantaneous inductor current
v_o	instantaneous output voltage
v_d	instantaneous diode forward voltage
v_{in}	instantaneous input voltage
v_{con}	instantaneous control voltage
d	instantaneous ON time ideal duty ratio
D_p	steady state ON time duty ratio considering all the resistive parasitics
C	capacitor
L	inductor
R	load resistance
r_C	ESR of capacitor
r_L	ESR of inductor
r_d	diode forward resistance
r_{dson}	MOSFET ON resistance
R_s	sensed resistance
S_f	OFF time slope of the sensed inductor current
S_n	ON time slope of the sensed inductor current
S_e	slope of the compensation ramp
R_{f1}	top feedback resistance
R_{f2}	bottom feedback resistance
C_a	compensator capacitance
C_b	compensator capacitance
R_a	compensator resistance
$G_{v_o d}$	output-to-duty-ratio transfer function
$G_{v_o v_{in}}$	output voltage-to-input voltage transfer function
$G_{v_o i_{load}}$	output voltage-to-load current transfer function
$G_{i_l d}$	inductor current-to-duty ratio transfer function
$G_{i_l v_{in}}$	inductor current-to-input voltage transfer function
$G_{i_l i_{load}}$	inductor current-to-load current transfer function
ω_c	gain crossover frequency
IC	integrated circuit
PID	proportional, integral and derivative
PCMC	peak current mode controller
SPICE	simulation program with integrated circuit emphasis
BW	bandwidth
Note:	For all the signals, small case italics are used to represent the instantaneous values, upper case for steady state values and small case italics with hat for small signal values.

process. Some other tuning approaches [4,5] modify the passive components in the compensator on a trial and error basis so as to meet the specifications. However, no direct relationship exists between the passive components and the desired specifications. All these approaches target a particular BW and PM without concentrating on the maximum achievable BW. A high BW is an attractive feature, since it invariably leads to faster time response. In this regard, the present work addresses an approach for compensator design with the aim of meeting the specifications related to PM, low frequency gain and GM and maximizing the BW. For this, the compensator design has been framed as an optimization problem that seeks to determine the compensator parameters that minimizes a given objective function.

Optimization techniques have been extensively applied to the design of DC–DC converters. Different objective functions are used to design power converter circuits that optimize a certain quantity of interest like efficiency, cost, size *etc.* under different constraints [6–10]. In [6], a monolithic DC–DC converter is designed that maximizes efficiency. Considering the nonlinear nature of the objective function and constraints, different nonlinear programming methods, particularly algorithms based on Lagrangian functions are used. Other notable studies in this regard include [7], where Lagrangian functions are used for optimization of a switched capacitor converter. In [8,9], optimization of DC–DC converters are carried out using augmented Lagrangian functions with penalty functions. A nonlinear programming method has been adopted in [10] to design boost-power-factor-corrector circuits. A Genetic Algorithm (GA) based approach for the design of power converters is formulated in [11].

In the only reported work on the application of optimization for compensator design of DC–DC power converters, a gradient based approach has been used to design Type-II compensator based only on the PM and BW specification by considering the non idealities of the op-amp [12]. Gradient based optimization techniques though quite fast and effective for simple objectives, suffers from the limitation of getting trapped into the local minima for certain complex nonlinear objective function.

Gradient free optimization techniques are broadly classified into two groups: local search based and evolutionary techniques. Local search based techniques, though computationally cheap (lesser execution time), suffers from the limitation of having very high probability of getting trapped into the local optimal point. Whereas, evolutionary optimization techniques have a far lesser probability of converging to the local optimal point. This has been the primary reason behind the emergence and wide applications of various heuristic based evolutionary optimization techniques like genetic algorithm (GA), particle swarm optimization (PSO), ant colony optimization (ACO) and differential evolution (DE) and cultural algorithms [13] in recent times. However, the improved convergence comes at the cost of a large number of function evaluations and hence high execution time. A number of works has been reported to overcome the limitations associated with evolutionary optimization techniques. In [14], a chaotic genetic algorithm with support vector regressions is proposed by incorporating chaotic movement of candidate solutions to maintain diversity in the population and avoid pre-mature convergence of the algorithm. Similarly, a number of variants of the standard PSO have been proposed, which aims at improving the convergence and accuracy of the final solutions obtained with standard PSO. These variants includes: Quantum PSO (QPSO) [15], PSO with Quantum Infusion (PSO-QI) [16], Adaptive inertia weight PSO [17], Craziness PSO (CRPSO) [18], dynamic PSO with quantum based local search [19].

The combination of local and heuristic search based optimization is known to incorporate the advantages of both, while offsetting their individual limitations, *i.e.* it provides faster to the global solution [20]. In this regard, a hybrid optimization based on the combination of particle swarm optimization (PSO) and Hooke Jeeves (HJ) has been proposed in [21]. The unconstrained approach has been applied for the design of a Proportional- Integral (PI) controller for prototype transfer functions based on a set of frequency domain (gain margin and phase margin) specifications only. In the present work, the hybrid approach is extended to add additional requirements on bandwidth and low frequency gain, and is further applied for the design of a fixed order compensator *i.e.* Type-II for DC–DC converter. The gain and phase margin requirements have been formulated as constraints in the objective function. In a recent work on the application of swarm optimization based approach for satisfying frequency domain specifications, an optimal linear phase FIR filter has been designed in [22].

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