



Original

## Digital counter cell design using carbon nanotube FETs

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### Abstract

Compressor and counter cells are the basic blocks used to accumulate the partial products in a multiplication process. In this paper, novel high speed and low power carbon nanotube counter cells are suggested. The efficiency of circuits is improved by using carbon nanotube field-effect transistors (CNFETs). The proposed designs are 4-to-3, 5-to-3, 6-to-3, and 7-to-3 counters. Using HSPICE, these proposed designs are simulated at different conditions. Simulation results confirm that the proposed designs are the fastest counters with lowest PDP in different working circumstance. © 2017 Universidad Nacional Autónoma de México, Centro de Ciencias Aplicadas y Desarrollo Tecnológico. This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>).

**Keywords:** Compressor; Counter cell; Carbon nanotube transistor; Multiplier

### 1. Introduction

Among the most basic blocks in computer arithmetic are multipliers, which are commonly used in different digital signal processors. In different applications of computing systems there is growing demands for high-speed multipliers, such as computer graphics, image processing, scientific calculation, and so on (Azarderakhsh & Reyhani-Masoleh, 2013; Bagherizadeh, Gerami, & Eshghi, 2014; Rodríguez-Reséndiz, Gutiérrez-Villalobos, Duarte-Correa, Mendiola-Santibañez, & Santillán-Méndez, 2012). The speed of a multiplier specifies how fast a processor will run. Designers are now more focused on low power consumption and high speed processors. A multiplication operation conventionally involves three operational stages: generation of partial products, reduction of partial products to two additive operands, and finally, carry propagation addition. The partial product reduction stage is respectful for a main part of the total multiplication delay, power and area (Waters & Swartzlander, 2010). Hence, in order to acquire partial products, compressor and counter cells usually implement this stage because they contribute to the reduction of the par-

tial products and the critical path (Jaberipur & Kaivani, 2009). Counters are much faster than conventional adders because they could act without carry signal along their digital stages. Counters are the basic blocks, which are used to acquire the partial products in the multiplication process (Deng & Chen, 2013). Thus, improving the power performance of these structures could lead to remarkable saving of the power used by the entire multiplier. Because of the miniaturization of the transistors, it is possible to increase the number used in each circuit. This nano level reduction will cause some acute problems such as short channel effects, remarkable gate control degradation and high leakage power consumption. A solution to these problems is using carbon nanotube field effect transistors (CNFETs) (Bagherizadeh & Eshghi, 2011a, 2011b; Perri & Corsonello, 2012). One of the most considerable properties of this type of transistor is the ability of having optional threshold voltage by changing the diameters of the nanotubes. This property makes CNFETs suitable for designing circuits with multiple threshold voltage ranges (Bagherizadeh & Eshghi, 2011a, 2011b).

In this paper, four novel high speed and low PDP CNFET-based counters are proposed. These counters are capable of adding four, five, six or seven bits per decade, and generate 3 outputs. CNFETs with different threshold voltages are used to design our proposed counters.

In the remainder of this paper, in Section 2, a brief review of the CNFET technology is presented. In the next section related

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works are discussed. The proposed CNFET-based counter cells are presented in Section 4. Experimental results, analyses and comparisons are presented in Section 5, and finally, Section 6 concludes the paper.

## 2. Carbon nanotube field effect transistors (CNFETs)

A carbon nanotube (CNT) is an allotrope of carbon with a tubal nanostructure. Transistors, which have carbon nanotubes as their channel, are called carbon nanotube field-effect transistors (Mehrabani & Eshghi, 2015). CNTs have particular properties that make them promising to be used in the field of integrated circuits. The most important and remarkable feature of CNFETs is their spectacular capability in current driving or current carrying, and experiments have shown that CNFETs are the best for this aim (Bagherizadeh & Eshghi, 2011a, 2011b; Lin, Kim, & Lombardi, 2009). Without any extra power overhead, CNFETs could operate five times faster than CMOS in the best case. Another fundamental feature of CNFETs is their varied behavior in manipulating the threshold voltage ( $V_{th}$ ) by adopting an appropriate diameter for CNTs (Bagherizadeh & Eshghi, 2011a, 2011b).

Multi-walled nanotubes (MWNT) consist of multiple rolled layers (concentric tubes) of graphite. A single-wall CNT consists of a tube-shaped wall which is made of graphite with the diameter of 1–2 nm. A multi-walled CNT has a thinner wall. The walls of the tubes are 34 nm each. The outer wall diameter of the multi-walled CNT is 2–25 nm (Mehrabani, Mirzaee, Moaiyeri, Navi, & Hashemipour, 2013).

A CNT is described by its chiral vector. The chirality vector is defined by an ordered pair  $(n_1, n_2)$  that characterize many electrical and physical properties of the carbon nanotube (Bagherizadeh & Eshghi, 2011a, 2011b; Mehrabi, Mirzaee, Zamanzadeh, Navi, & Hashemipour, 2013; Mehrabi, Navi, &

Hashemipour, 2013; Mehrabi, Mirzaee, Moaiyeri, et al., 2013). It is calculated using Eq. (1):

$$C_h = n_1 \hat{a}_1 + n_2 \hat{a}_2 \quad (1)$$

where  $[\hat{a}_1, \hat{a}_2]$  are the lattice unit vectors and  $n_1, n_2$  are positive integers which specify the tube's structure. The single-walled carbon nanotubes (SWCNT) could be a metal or a semiconductor, if  $n_1 - n_2 \neq 3k (k \in \mathbb{Z})$ , then the SWCNT is a semiconductor; otherwise it is a metal.

The diameter of the CNT is calculated using Eq. (2) (Alkaldy, Navi, & Sharifi, 2014; Bagherizadeh & Eshghi, 2011a, 2011b; Mehrabani & Eshghi, 2015).

$$D_{CNT} = 0.0783 \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

The threshold voltage of a CNT channel is approximated as the inverse function of diameter and could be computed as Eq. (3). A special threshold voltage of a CNFET could be obtained by a suitable diameter (Alkaldy et al., 2014).

$$V_{th} \approx \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{a V_\pi}{e D_{CNT}} \approx \frac{0.43}{D_{CNT}} \quad (3)$$

where parameter  $a$  ( $\approx 0.249$  nm) is the carbon-to-carbon atom distance,  $V_\pi$  ( $\approx 3.033$  eV) is the carbon  $\pi$ - $\pi$  bond energy in the tight bonding model, and  $e$  is the unit electron charge,  $E_g$  is the band gap, and  $D_{CNT}$  is the CNT diameter.

There are three kinds of CNFET: The first kind is the MOSFET-like CNFET (which contains the p-type CNFET and n-type CNFET), which operates in a unipolar mode; the second kind is the Schottky barrier (SB) CNFET, which shows ambipolar characteristics, but because of the SB element, it is not appropriate for high performance applications; the third kind of CNFET, suitable for low power applications, is the band-to-band tunneling CNFET that has obviously low current in its active mode (Alkaldy et al., 2014). Fig. 1 shows three kinds of

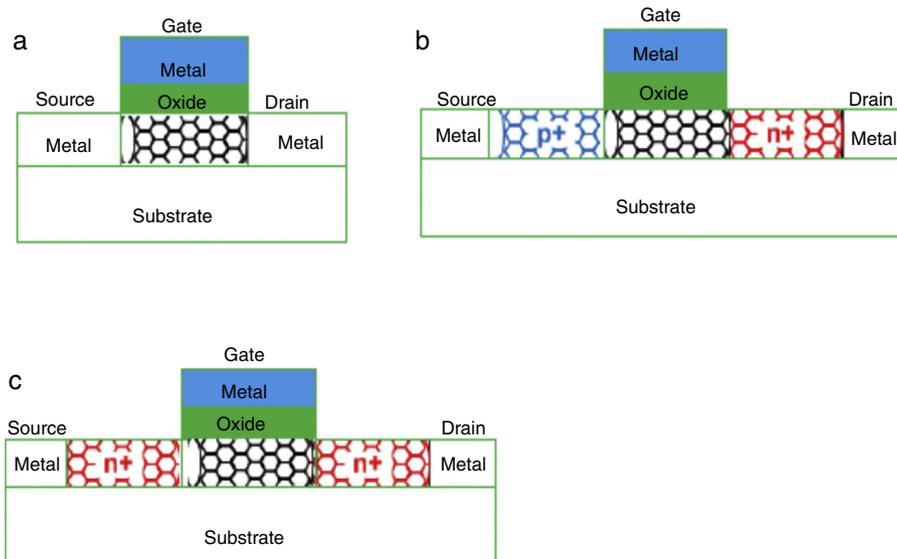


Fig. 1. (a) SB-CNFET, (b) T-CNFET, and (c) MOSFET-like CNFET.

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