Materials Science in Semiconductor Processing #vol# (xxxx) xxxx–xxxx

Contents lists available at ScienceDirect

Materials Science in Semiconductor Processing

journal homepage: www.elsevier.com/locate/mssp

Doping top-down e-beam fabricated germanium nanowires using molecular monolayers

B. Long[a,b,*], G. Alessio Verni[a,b], J. O'Connell[a,b], M. Shayesteh[a], A. Gangnaik[a,b], Y.M. Georgiev[a,b], P. Carolan[a], D. O'Connell[a], K.J. Kuhn[d,1], S.B. Clendenning[d], R. Nagle[a], R. Duffy[a], J.D. Holmes[a,b,c]

[a] Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland
[b] Materials Chemistry & Analysis Group, Department of Chemistry, University College Cork, Ireland
[c] Advanced Materials and BioEngineering Research (AMBER), Trinity College Dublin, Dublin 2, Ireland
[d] Components Research, Intel Corporation, Hillsboro, Oregon, USA

ARTICLE INFO

Keywords:
Molecular layer doping
Nanowires
Semiconductors
Germanium
Conformal
Non-destructive

ABSTRACT

This paper describes molecular layer doping of Ge nanowires. Molecules containing dopant atoms are chemically bound to a germanium surface. Subsequent annealing enables the dopant atoms from the surface bound molecules to diffuse into the underlying substrate. Electrical and material characterization was carried out, including an assessment of the Ge surface, carrier concentrations and crystal quality. Significantly, the intrinsic resistance of Ge nanowires with widths down to 30 nm, doped using MLD, was found to decrease by several orders of magnitude.

1. Introduction

State-of-the-art microprocessors contain several billion transistors over a ~6 cm^2 area [1]. This enormous device density has been made possible by continuous transistor scaling. However, in the last 10–15 years issues, such as increased leakage current, directly related to device scaling, [2] have necessitated radical changes in fabrication procedures, one of which has been the need to transition from planar to non-planar device architectures [3].

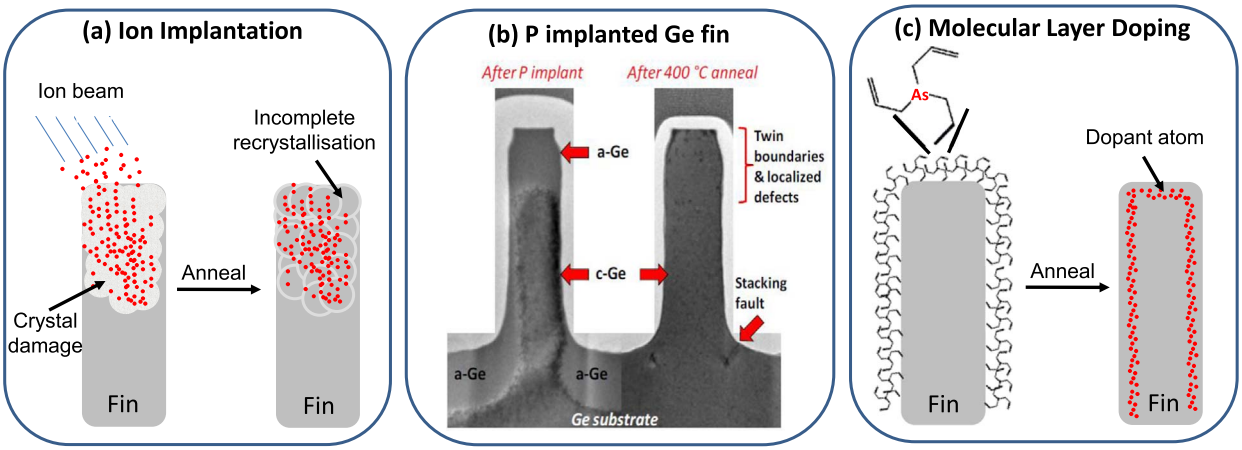
Traditional architectures, with planar bulk substrates and highly doped channels for short-channel-effect control became problematic due to scaling, necessitating the development of non-planar devices (*e.g.* multigate FETs such as FinFETs). These architectures enabled better switching control, minimizing leakage current issues. Unfortunately, standard industrial techniques for doping, *e.g.* ion implantation, were designed for the former [4]. Doping, or the introduction of impurity atoms, a fundamental process step in the fabrication of integrated circuits, allows tuning of the electrical properties of the semiconductor material. Ion implantation, however, is destructive to the crystal structure of the semiconductor and too mono-directional for modern device architectures. These problems are depicted graphically in Scheme 1(a). A TEM cross-section of a Ge fin that has been implanted with P is shown in Scheme 1(b). Amorphisation of the crystal structure of the target substrate is normal after implantation but subsequent high temp annealing induces recrystallization. On planar substrates this was satisfactory however for non-planar device architectures, residual defects, such as twin boundaries, remain. Furthermore, as the fin width decreases further complete recrystallization, even with defects, will not be possible [5].

Molecular layer doping (MLD), pioneered by the Javey Group [6] has been shown to non-destructively dope planar Si substrates. Since then a number of III-V materials have been doped using molecular layers [7–10]. MLD is based on surface functionalization and has the potential for precise atomistic control of the dopant position and composition on the surface of a semiconductor (as depicted in Scheme 1 (c)). Thermal decomposition of this molecular layer enables the freed-up dopant atoms to diffuse into the underlying semiconductor. Furthermore, minimal damage to the crystal structure of this substrate occurs, due to the gentle nature of the process.

As well as exploring new methods for doping, new materials with higher carrier mobilities than Si are also being investigated. To date improved performance has been achieved mostly through transistor scaling with the economic benefit of reusing existing infrastructure. For this trend to continue moving to a high carrier mobility material which can enable reduced power consumption (by delivering a fixed drive current and circuit speed at a reduced power supply voltage) is a priority. Materials such as graphene, [11] transition metal dichalcogenides (TMDs) [12] and III-Vs [13] are being considered. Germanium

* Corresponding author at: Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland.
E-mail addresses: brenda.long@ucc.ie, brenda.long@ucc.ie (B. Long).
[1] Current Department of Materials Science and Engineering, Cornell University, Ithaca, NY, USA.

http://dx.doi.org/10.1016/j.mssp.2016.10.038
Received 25 July 2016; Received in revised form 17 October 2016; Accepted 20 October 2016
Available online xxxx
1369-8001/



Scheme 1. (a) Depiction of ion implantation and associated problems for small dimension fin structures, (b) cross sectional TEM of ion implanted Ge fin pre- and post-anneal indicating presence of residual defects in recrystallized structure and (c) depiction of MLD as a process that will overcome problems associated with ion implantation.

(Ge), however, is a particularly attractive replacement for Si due to its enhanced electron and hole mobilities, and CMOS (complementary metal oxide semiconductor) compatibility, allowing Ge to be processed on existing Si technology platforms. Recent progress of ultra-shallow doping of n-type Ge using phosphorus has included several works using phosphine, as well as tunable δ-doping with near-monolayer P using P_2 [14–18]. However these works were based on doping planar surfaces, and to the best of our knowledge were not yet transferred to nanowire device applications.

In general, processing and chemical techniques employed by Si are broadly transferrable to Ge, however, due to the unstable oxide of Ge, the surface chemistry is vastly more challenging. This study focuses on MLD of Ge with arsenic for a variety of reasons: 1) the relatively high equilibrium solubility of arsenic in Ge and 2) arsenic ability to in-diffuse in Ge. In this research, molecules containing arsenic were chemically bound in self-limiting monolayers to Ge surfaces resulting in doped substrates after annealing. Material characterization showed that the integrity of the surface was maintained and the underlying crystal structure was not damaged, while electrical characterization showed several orders of magnitude decrease in resistance.

2. Materials and methods

All chemicals, purchased from Sigma-Aldrich were reagent grade and used as received. All experiments on unpatterned substrates were carried out on Ge(100) wafers purchased from Umicore, These substrates had p-type doping in the concentration range of $5–9\times10^{16}$ at/cm^3. The nanowire samples were fabricated from undoped (100) germanium-on-insulator (GeOI), with a Ge thickness of 50 nm.

2.1. Material and electrical characterization

Atomic force microscopy (AFM) was implemented in tapping/non-contact mode at room temperature over a 3×3 μm scanning area. Cross-sectional transmission electron microscopy (TEM) was carried out using JEOL 2100 HRTEM operated at 200 kV. Cross-section samples were obtained by using FEI's Dual Beam Helios Nanolab system. For electrical characterization Keithley 37100 and Keithley 2602 parameter analyser were used. Secondary ion mass spectrometry (SIMS) was performed on doped samples to obtain the total dopant concentration. SIMS analysis typically has a standard error of 20% in concentration and a 10% relative error from sample to sample. SIMS analysis was carried out on a CAMECA IMS 4FE6 system, available at the UMS-CNRS Castaing Characterization Centre in Toulouse. Electrochemical capacitance voltage (ECV) profiling was used to determine the active carrier concentration in doped samples, using thiron as the etchant. The technique uses an electrolyte-semiconductor Schottky contact to create a depletion region, which behaves like a capacitor. The measurement of the capacitance provides information of the electrically active doping densities. Depth profiling is achieved by electrolytically etching the semiconductor between the capacitance measurements. The process is repeated for multiple steps, generating a carrier profile. It is a destructive technique, as there is a crater on the sample after the measurement is finished. No special test structure is required, it is performed on an unpatterned surface. For ECV data presented here, errors did not exceed 20%. X-ray photoelectron spectroscopy (XPS) was carried out with a VG Scientific Escalab MKII system using Mg X-rays at 1253 eV. Survey scans were performed using a pass energy of 200 eV and core level scans at a pass energy of 20 eV.

2.2. MLD procedure

Synthesis of triallyarsine (TAA) was carried out using a published procedure [19]. As TAA is a toxic material it should be handled with care using adequate PPE. Due to its unstable nature it must be stored in an inert atmosphere while minimizing its exposure to air during transfer.

2.2.1. Substrate preparation

Ge was degreased by sonicating in acetone for 180 s, rinsed in IPA and dried under a stream of nitrogen, before being immersed in a 10% HF solution for 10 min, removed and dried under a stream of nitrogen. Ge was prepared immediately prior to reaction with TAA to minimize any possible re-oxidation.

2.2.2. Reaction of TAA with Ge

A solution of TAA in IPA (1:5) was degassed using 3× freeze/thaw cycles and transferred to a quartz flask containing the clean Ge substrate. The sample was irradiated for 2 h with UV light (λ=254 nm) after which it was removed and rinsed several times with IPA and acetone. All functionalization experiments were carried out in an inert atmosphere.

2.2.3. Capping layer deposition

SiO_2 capping layers were deposited used three different methods: 50 nm of oxide was sputtered, evaporated or deposited using CV538+53D. The annealing step was carried out in the presence if these oxides, after which they were removed using a standard BOE etch.