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Etch-free addressable organic sensor arrays

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ABSTRACT

Using a direct UV fabrication technique, an organic transparent 8×8 capacitive touch screen panel has been designed, fabricated and characterized. The active electrode material is poly(3,4-ethylenedioxythiophene): poly (styrenesulfonate) (PEDOT:PSS). The UV process provided spatial control over the PEDOT:PSS film conductivity, which was subsequently used to fabricate the touch screen panel. This process does not require external photoresists or secondary development and etch steps. The UV patterning of PEDOT:PSS provided a 3-order-of-magnitude reduction in material conductivity between exposed and unexposed regions. Spatial location of touch events can be accurately identified by monitoring relative changes in capacitance at each of the individual elements of the array. A typical touch event causes a measured capacitance reduction of ~100 fF at the touched intersection. The tested devices exhibit high optical transmission exceeding 80% across the visible spectrum. This technology allowed the device to be realized in a single processing step that is amenable to large scale, high-throughput organic fabrication techniques such as roll-to-roll processing.

1. Introduction

The spiraling appeal and associated demand for lighter, cheaper, and thinner electronic devices have fueled the utilization of organic and polymer materials in emerging generations of electronic circuits [1]. The adoption of these materials in electronics has several advantages including physical flexibility, semi-transparent devices, and the economics of roll-to-roll manufacturing.

In the area of transparent capacitive touch screen panel (TSP) technologies, existing design strategies have regularly used indium tin oxide (ITO) as the primary electrode material. This is because ITO, a transparent conducting oxide, has outperformed other inorganic materials. This is due to its low-temperature deposition, high conductivity and ease of etching. However, ITO suffers from limitations including brittleness, high material cost and vacuum deposition requirements [2]. The loss of electrical performance due to its brittle nature has been acknowledged for over a decade [3]. In order for TSP technologies to be compatible with high-throughput scalable organic electronics produced using roll-to-roll methods, the aforementioned limitations must be circumvented.

There is a pressing need for alternatives to ITO to be developed. The search for a suitable transparent electrode replacement has expanded to non-traditional materials such as silver nanowires, organic polymers, graphene, and carbon nanotubes [4–10]. A common challenge associated with many of these replacement materials is the lack of suitable patterning techniques that afford high-throughput capabilities. Common across all previous demonstrations, regardless of material, is the requirement for the transparent electrode to be amenable to patterning using a variety of micro- or nanofabrication techniques. However, such patterning often requires secondary photoresists, etchants and caustic environments that may preclude integration with underlying organic and CMOS-based devices.

The use of conductive organic polymers as electrodes is becoming increasingly popular. This is not only due to their desirable material properties such as mechanical flexibility, but also because their deposition techniques are intrinsically compatible with organic devices. In particular, poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) (PEDOT:PSS), a commercially available organic conductor, is attracting interest due to its solubility in water, relatively high conductivity, and environmental stability in comparison to other organic materials [11].

Several fabrication techniques have been previously used to realize capacitive TSPs using PEDOT:PSS including inkjet printing, laser ablation and micromolding; however, only inkjet printing has reported the realization and characterization of a working device [12–14]. Of the reported demonstrations, only micromolding is truly compatible with scalable high-throughput fabrication, whereas both individual inkjet printing and laser ablation approaches are serial patterning processes.

As such, there remains a real need and an unmet demand for materials and associated fabrication processes that can replace ITO

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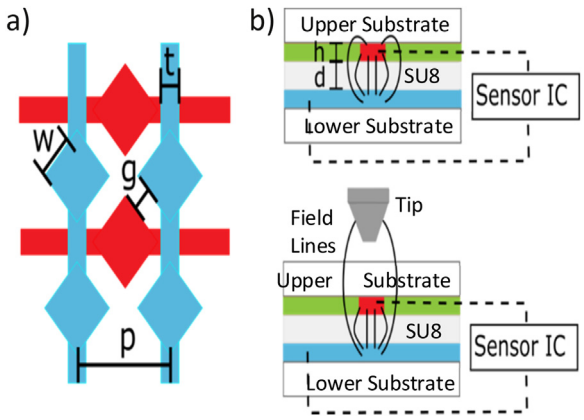

Fig. 1. a) Schematic of electrode design with interlocking diamond structure. The vertical and horizontal electrode lines (blue and red respectively) reside at different heights within the device. b) A schematic depiction of the fields associated with mutual capacitance sensing, showing the shunting of the electromagnetic fields between electrode pads upon introduction of a conductive stylus (bottom). The electrical connections to the sensing electronics are also shown. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

while mitigating the aforementioned drawbacks to enable competitive, inexpensive organic electronic devices. It is crucial that in order to create commercially viable technologies, the materials and fabrication process be compatible with large scale, high throughput processing such as roll-to-roll methods.

In this work, a fabrication process and the associated device architecture for mutual-capacitance organic PEDOT:PSS-based TSPs with high spatial resolution is proposed, demonstrated, and characterized. The devices are realized using a novel processing technique that selectively tailors the material conductivity in the planar spatial dimension by utilizing a UV-induced polymer scission process. In contrast with other patterning mechanisms, direct UV scission does not have any inherent material compatibility constraints. The technique has been developed, characterized and implemented to pattern the output emission of an organic light emitting diode [15]. This direct, etch-free spatial patterning technique is compatible with scalable, high-throughput and roll-to-roll manufacturing, where it is spatially limited only by the critical dimension of the UV shadowmask.

2. Capacitive touch sensor panel design

To demonstrate the application of the etch-free patterning technique, a commonly used TSP electrode layout, is designed and adopted for the devices reported within. Due to the relatively low sensitivity of the employed mutual capacitive sensing technique, an interlocking diamond parallel-plate structure shown in Fig. 1a) has been designed to increase the fringing field between electrodes. The row and column electrodes shown in Fig. 1a) are fabricated on separate substrates and isolated using a dielectric medium as shown in Fig. 1b). For such a design, the measured capacitance between a specified row and column electrodes can be expressed as [16]

$$C_{\text{element}} = \frac{t^2\varepsilon}{d} + \frac{8\pi w\varepsilon}{\log(\frac{4d}{h})}, \quad (1)$$

where t is the electrode trace width, ε is the permittivity of the dielectric interlayer, d is the thickness of the dielectric, h is the thickness of the electrode material, and w is the length of the side of the diamond. The fabricated structure has values of $t = 0.5$ mm, $w = 0.9$ mm, $g = 0.5$ mm, $h = 100$ nm, $d = 5$ μm, $p = 2.5$ mm, and $\varepsilon = \sim 4\ \varepsilon_0$. Together with Eq. (1), these give an estimated value of 1.92 pF for the unperturbed capacitance between a row and column electrode.

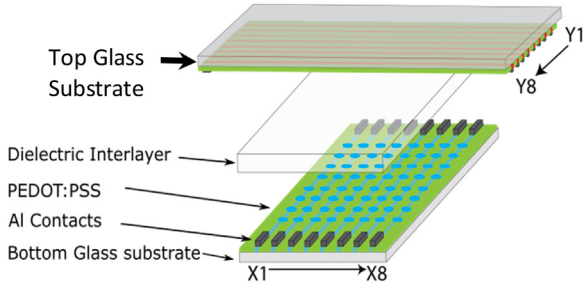

Fig. 2. Generalized assembly of the 8 × 8 capacitive sensing array made from dual UV-patterned substrates, allowing for addressable contact to each of the 64 capacitive elements.

In comparison to ITO panels which often implement electrodes with a trace width of 20 μm, a wider 0.5 mm trace is required due to the relative lower conductivity of PEDOT:PSS. This results in a larger crossing overlap between the rows and columns, thereby sacrificing some of the spatial sensitivity in order to allow for high conductivity through the unexposed PEDOT:PSS trace. The lower conductivity of PEDOT:PSS also makes it necessary to deposit metal contacts on opposing edges of the capacitive sensor to ensure that, during bias while sensing, a minimum resistance from the trace to the element under test is maintained.

The sensors demonstrated here consist of 8 individually addressable rows and columns, effectively creating 64 separate capacitive sensing elements. With the parallel-plate interlocking diamond structure, the mode of operation is based on sensing the mutual capacitance between the row and column traces. When a conductive stylus or human finger is near or in contact with the top glass substrate, a portion of the fringing field lines is shunted away from the mutual capacitors between the X and Y traces with a subsequent change in capacitance as shown in Fig. 1b) [16].

The spatial definition of the PEDOT:PSS electrodes in the capacitive sensor is achieved by using a direct UV patterning technique. As opposed to traditional methods of physically defining separated TSP electrodes, this novel fabrication technique selectively modulates the conductivity of regions within the thin film by up to 4 orders of magnitude when compared to the pristine polymer [15]. This approach allows new capabilities of for micron-scale precision patterning of electronic devices in a single processing step without the requirement of additional deposition, development, or etch steps.

3. Methods and materials

PEDOT:PSS was spun onto cleaned boroaluminosilicate glass slides. The resultant film thickness was approximately 100 nm prior to UV exposure. The films were irradiated by a Spectroline XL-1500 Crosslinker through an electroformed Ni shadow mask. A total exposure energy of 75 J/cm^2 at 254 nm was irradiated onto the films. Following the UV patterning, aluminum contacts were thermally evaporated onto both ends of the PEDOT:PSS electrodes. Employing this direct UV exposure patterning necessitated a design in which the row and column electrodes are separated by a dielectric interlayer. The capacitive array is comprised of two identically patterned PEDOT:PSS films that are oriented 90° with respect to each other and secured using an SU8 interlayer. The SU8 interlayer was spun onto one of the substrates using SU8 2000.5 at a final spin speed of 3000 RPM resulting in an approximate thickness of 5 um. Upon appropriate alignment of the top substrate, the completed device was then baked at 60 °C for 1 h under a 1 kg weight to ensure appropriate adhesion of the substrates. The generalized design and of the capacitive structure is shown in Fig. 2. It should be noted that the individual diamond structures patterned on each conductive