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Leakage current conduction in metal gate junctionless nanowire transistors

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ABSTRACT

In this paper, the experimental off-state drain leakage current behavior is systematically explored in n- and p-channel junctionless nanowire transistors with HfSiON/TiN/p^+-polysilicon gate stack. The analysis of the drain leakage current is based on experimental data of the gate leakage current. It has been shown that the off-state drain leakage current in n-channel devices is negligible, whereas in p-channel devices it is significant and dramatically increases with drain voltage. The overall results indicate that the off-state drain leakage current in p-channel devices is mainly due to trap-assisted Fowler-Nordheim tunneling of electrons through the gate oxide of electrons from the metal gate to the silicon layer near the drain region.

1. Introduction

Junctionless nanowire transistors (JNTs) have been considered as promising devices to extend the scaling limit to lower channel lengths, avoiding ultra-high doping concentration gradients at the source/drain junctions [1]. Compared to junction-based nanowire transistors, they offer lower off-state current, near ideal subthreshold slope and less mobility degradation with gate voltage [1]. However, the on-state drain current of JNTs is lower than that of the inversion mode devices [2] and, therefore, the off-state leakage current is of great significance for these devices.

Several works are referred in previous literature regarding compact models for the drain current in the on-state region [3–6] and leakage current investigation in the off-state region of JNTs [7–12]. In particular, the effect of longitudinal band-to-band tunneling (BTBT) from the channel to the drain on the off-state behavior of silicon-on-insulator (SOI) and bulk planar JLTs [7], vertically stacked nanowire JNTs [8] and dual-material gate nanowire JLTs [9,10] have been studied with numerical simulations to optimize the ON-to-OFF current ratio. However, unlike the studies of previous work based on numerical simulations [7–10], experimental investigations of the leakage current in JNTs showed different or additional conduction mechanisms. In p-channel germanium nanowire JNTs with HfO_2 gate dielectric, it has been demonstrated that in addition to BTBT, the off-state leakage current is affected by the Shockley-Read-Hall generation and trap-assisted tunneling mechanisms [11]. The off-state leakage current has been analyzed also in both n- and p-channel multi-fin silicon JNTs with HfSiON/TiN/polysilicon gate stack of equivalent oxide thickness (EOT) 1.5 nm and doping concentrations 5×10^{18} and 1×10^{19} cm^{-3} [12]. The experimental bias and temperature dependent leakage current data were explained considering trap-assisted tunneling in both types of JNTs with traps located along the entire interface between silicon/gate dielectric, coexisting with direct tunneling through the gate dielectric [12].

In this article, we have systematically explored the off-state leakage current in n- and p-channel JNTs with HfSiON/TiN/p^+-polysilicon gate stack of equivalent oxide thickness (EOT) 1.2 nm. In relation to reference [12] where the off-state leakage current has been analyzed in both n- and p-channel nanowire silicon JNTs with 50 parallel fins, we have investigated isolated single-fin devices of similar technology with a different source and drain architecture as described in Section 2, showing distinctive differences in the leakage current behavior. In particular, the experimental results showed that the off-state leakage current is insignificant

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in n-channel devices, which is unlike the behavior observed in [12]. In the p-channel nanowire silicon JNTs, the strong bias and the weak temperature dependent leakage current data are explained by Fowler-Nordheim (F-N) tunneling of electrons from the metal gate to the silicon layer. Furthermore, measurements of the off-state leakage current at the source and drain electrodes, as well as its dependence on the channel length indicate that the tunneling occurs in a region near the drain contact. Finally, the off-state leakage current is quantitatively analyzed in the p-channel JNTs, from which the barrier height between TiN/HfSiON is extracted and the physical interpretation for negligible leakage current in the n-channel JNTs is presented. Guidelines to reduce the off-state leakage current are proposed. It is noted that the fin height and width are larger than 5 nm, so that the quantum confinement effects can be reasonably neglected [13].

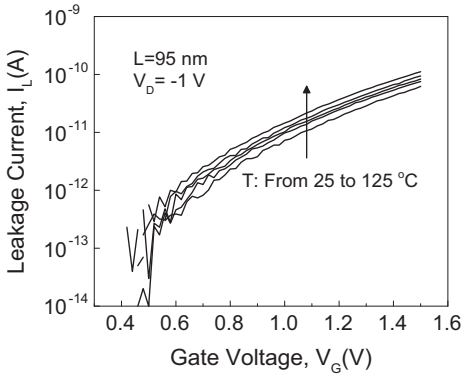

Fig. 2. Leakage current as a function of the gate voltage at different temperatures of p-channel JNT with channel length L = 95 nm, measured at drain voltage $V_D = -1$ V.

2. Experimental details

The measured JNTs were fabricated at CEA-LETI on (100) SOI wafers with 145 nm thick buried oxide (BOX) [14]. After thinning the Si body down to about 10 nm, a full-sheet implantation was carried out before active patterning with a phosphorus or boron doping targeted at 2×10^{19} cm^{-3}. The high-k-metal gate stack is composed of HfSiON/TiN/p$^+$-polysilicon, with an EOT of 1.2 nm. The TiN metal gate used was featuring a work function close to mid-gap. Using a nitride spacer on the sidewalls of the gate, an additional implantation was performed to source/drain regions in order to improve electrical performance by reducing access resistance, resulting in source/drain doping level $\approx 10^{20}$ cm^{-3}. The channel length L is varying from 25 to 95 nm, the fin height is H_{fin} = 10 nm and the fin width is W_{fin} = 18 or 26 nm for the n- and p-channel JNTs, respectively. It is mentioned that the leakage current increases with W_{fin} as a result of the gate area increase [12]. Drain current measurements were performed using the Agilent B1500/1530 Semiconductor Device Analyzer. The measuring limit of the analyzer is around 10^{-13} A.

3. Results and discussion

Fig. 1(a) and 1(b) shows typical I_D-V_G characteristics of n- and p-channel JNTs with channel length L = 95 nm, measured at different drain voltages V_D. In the n-channel JNT, the measured off-state leakage current is negligible corresponding to the measurement limit of the analyzer. In the p-channel JNT, the off-state leakage current increases dramatically when $|V_D|$ increases from 0.4 to 1 V, which indicates the occurrence of a tunneling conduction [15]. This is supported with the results of Fig. 2, showing that the gate current is substantially independent of temperature, in agreement with the results of a previous work on MOSFETs with HfSiON gate stack [16].

In order to identify the origin of the off-state leakage current observed in p-channel JNTs, in Fig. 1(b) the absolute gate current (I_G) and the drain current (I_D) are plotted versus V_G for different drain voltages. It is worth mentioning that in both types of JNTs, the on-state gate current is negligible compared to the drain current and it is not evaluated. In the p-channel JNT, the magnitude of the off-state drain current is similar to the gate current showing that carriers tunnel between metal gate and silicon layer through the gate dielectric, in agreement with the finding of previous work [12]. However, the I_D-V_G characteristics measured simultaneously at the source and drain electrodes show that the off-state leakage current is significant at the drain electrode and negligible at the source electrode as shown in Fig. 3(a). This result indicates clearly that the channel region where the tunneling occurs is located near the drain region.

Moreover, the gate current measured at $V_D = -1$ V and V_G = 1.5 V is almost independent of the gate length as shown in Fig. 3(b), which also indicates that the leakage is occurring in a region close to the drain. It is noted that the off-state gate current is positive in p-channel JNTs, indicating that electrons tunnel from the metal gate to the silicon layer, since tunneling of holes from the silicon layer cannot occur because the channel of the JNT is fully depleted in the off-state region.

The voltage drop across the gate dielectric V_{ox} is expressed as:

$$V_{ox} = V_G - V_{FB} - \phi_{s,drain}, \quad (1)$$

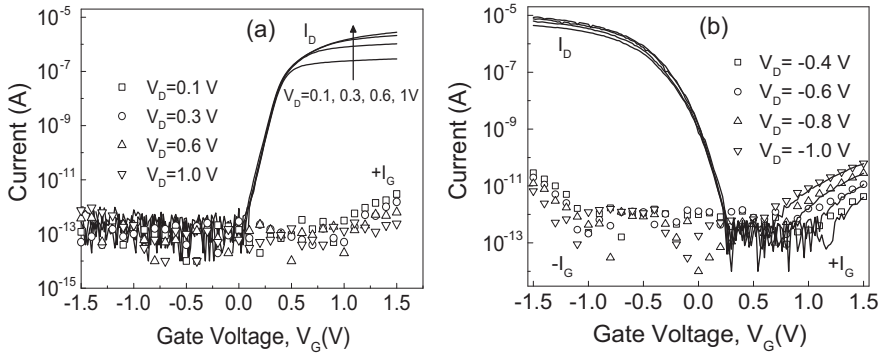

Fig. 1. Drain current I_D versus gate voltage V_G (solid lines) and gate current I_G versus gate voltage V_G (symbols) of n-channel (a) and p-channel (b) JNTs with channel length L = 95 nm, measured at different drain voltages.