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# Simultaneous switching noise reduction by resonant clock distribution networks

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ABSTRACT

Resonant clock distribution networks are known as low-power alternatives for conventional power-hungry buffer-driven clock networks. In this paper, we investigate the simultaneous switching noise (SSN) in a resonant clock network compared to that in conventional clocking. Analytical and simulation results show that employing the clock generated by a resonant clock network reduces the SSN voltage on power supply rails. The main drawback of using a sinusoidal clock is that the short-circuit power increases in the clocked devices. This problem is also investigated and discussed analytically.



## 1. Introduction

The trend of increasing complexity, speed and density in today's very large scale integrated (VLSI) circuits, due to aggressive technology scaling, introduces new challenges in design and fabrication process. As an example, in today's microprocessors with millions of transistors, a conventional buffer-driven clock tree is typically utilized to synchronize all the elements connected to the leaves. Due to employing high clock frequencies, fast and sharp clock edges are applied to the clocked devices. In such a synchronization scheme, these sharp clock edges occur at the same time creating large current pulses in the power distribution network (PDN). These large and fast current variations flow through on-chip parasitic inductance inherent to the power rails and also off-chip bonding wires resulting in unwanted voltage fluctuations ($L \cdot di/dt$) which is known as simultaneous switching noise (SSN).

The generated SSN can create serious problems in signal/power integrity [1]. Furthermore, it is considered as one of the important sources of on-chip electromagnetic interference (EMI) [2–5]. Nowadays, since in many applications electronic circuits are playing a crucial role, electromagnetic compatibility (EMC) issue becomes a serious liming factor.

Many techniques have been proposed to suppress SSN in a clocking network. Using multiple bonding wires in order to reduce the total inductance to decrease the value of $L \cdot di/dt$ is one way to reduce the SSN. In this technique, we need to consider the relative placement of pins carefully, as the absolute value of the inductance is not the only important factor [6]. In [7], a method to determine the optimum number of pins is presented. Furthermore, advance packaging methods can be used to reduce the inductance value [8,9]. However, these methods increase the total packaging costs.

In order to suppress SSN, another method is to distribute clock edges within a specific timeslot, as long as it is allowed by timing constraints [10]. This helps to prevent simultaneous occurrence of clock edges. However, this technique is not directly supported by CAD tools and also proper clock drivers need to be utilized in order to employ this method.

Another effective technique to suppress SSN is to insert on-chip and off-chip decoupling capacitors (i.e., decaps) [11]. Effectiveness of this technique has been studied and analyzed in [12]. Although decoupling capacitors exhibit capability of SSN suppression, they are not area efficient. Due to this fact, careful optimization is required to choose the proper capacitance size to avoid extreme area penalties.

As mentioned earlier, fast clock edges increase the switching noise by increasing $di/dt$. Hence, one low-cost solution to reduce SSN is to employ a signal with relaxed rise and fall time (i.e., slower edges) [13–15]. Obviously, this technique creates some difficulties in management of timing budget for high-speed applications. However, in [14] and [15], about 40–60% noise reduction has been reported by accepting some speed penalty.

In this paper, we investigate a new SSN reduction technique based on resonant clock distribution, which has been previously proposed as a low-power alternative for the conventional buffer-driven clocking [16–19]. In this clocking strategy, since a sinusoidal clock is generated for the clock distribution purpose, the peak

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energy of higher harmonic components is suppressed significantly, resulting in smoother transitions. An analysis is presented in this work in order to show the great capability of resonant clocking in SSN reduction. Furthermore, other issues associated with resonant clocking such as effect of harmonic distortion on SSN and short-circuit power dissipation problem are investigated.

The organization of this paper is as follows. In Section 2, the basics of resonant clocking are presented. Section 3 is dedicated to comparison of SSN in resonant clock distribution and conventional buffer-driven clocking. In Section 4, effect of harmonic distortion in resonant clocking on SSN is discussed. Then, the short-circuit power dissipation issue is investigated in Section 5 followed by results and comparison in Section 6 and conclusions in Section 7.

## 2. Basics of resonant clocking

The clock distribution network in a VLSI circuit (e.g., a microprocessor) can be divided into global and local clock distributions [16]. The global network consists of the clock source and buffer stages which connect the clock source to the logic gates by wires and interconnects, while the local network consists of the final load and associated wires which connect them to the final buffer stage. Fig. 1(a) shows a simplified model of a conventional buffer-driven clock distribution network. The main idea behind a resonant clock distribution network is to use the clock capacitance to render oscillation using *LC*-based oscillators [16–19]. A simplified model of this clocking strategy is shown in Fig. 1(b). A resonant clock can be delivered globally to the leaf node clock buffers using distributed oscillators [19], or alternatively, to gain the maximum power savings, it can even be distributed completely bufferless directly to the clocked elements [16–18]. In either of these methods, a sinusoidal clock is generated and delivered to devices, which are connected to clock network directly or through local buffers. In terms of clock power dissipation, it can be proven that

$$\frac{P_{res}}{P_{conv}} = \frac{3\pi(n-1)}{4nQ_{tank}} \tag{1}$$

where $P_{res}$ and $P_{conv}$ are the clock power dissipation in the resonant clocking and the conventional clocking, respectively, $n$ is the tapering factor in the conventional clocking, and $Q_{tank}$ is the quality factor of the *LC* tank utilized for the clock generation in the resonant clock distribution network [16]. As a numerical example, for $n=3$, a tank quality factor higher than $\pi$ would result in more than 50% clock power saving by using resonant clocking scheme.

In the previous studies on the resonant clock distribution networks, the main focus were on clock power saving capability of this clocking strategy [16–19]. Hence, the application of a resonant clocking network has always been limited to high-speed processors in which the clock power dissipation is a considerable fraction of the total power dissipation. It has barely been considered for other potential applications where the power consumption is not the primary concern. Due to this reason, there have not been sufficient studies about other possible applications of resonant clocking networks. In [20], it has been shown that the total radiated EMI can be reduced significantly by utilizing this clocking strategy. In this paper, we move further to reconsider and demonstrate this technique for other new applications. We investigate the switching noise performance of a resonant clock distribution network and discuss different design issues and considerations. Furthermore, we present a comparison of short-circuit power dissipation in resonant and conventional clocking, in order to get more insight about the trade-offs involved in employing this clocking strategy in the future applications.

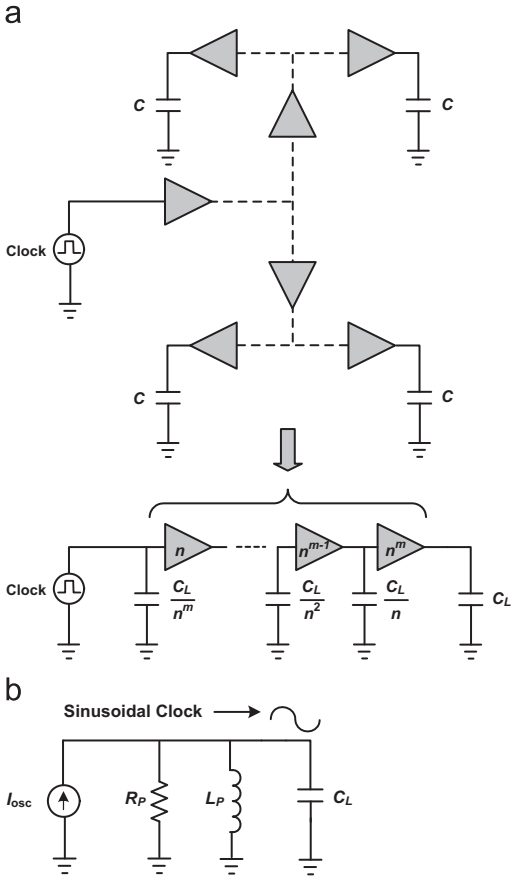


**Fig. 1.** A simplified model of (a) a buffer-driven clock network, and (b) a resonant clock distribution network.

## 3. SSN in resonant clocking

### 3.1. Basic considerations

In power supply rails, the parasitics contributed by wires, interconnects, transistors, etc. form *RLC* circuits which are the source of undesired voltage fluctuations. To have a basic understanding about the phenomenon, let us consider the simple circuit shown in Fig. 2. In this figure, an AC current is injected through a current source into an ideal inductor.

We investigate two different cases. For the first case, we assume that the injected current has a trapezoidal shape varying between 0 and $A$ with identical rise and fall times (i.e., $t_r$). The maximum $di/dt$ occurs during the rising and falling edges creating a voltage change across the inductor which equals to

$$V_{L,\max} = L\frac{di}{dt}\Big|_{\max} = \frac{AL}{t_r}. \tag{2}$$

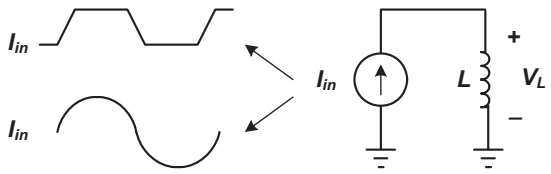


**Fig. 2.** An ideal inductor is fed by a current source.