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Research paper

The fabrication of carbon nanotube electronic circuits with dielectrophoresis

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ABSTRACT

Single-walled carbon nanotubes (SWCNTs) are used widely in fabricating nanoelectronic devices because of their unique electrical properties. In this paper, we report the fabrication of carbon nanotube field-effect transistors (CNTFETs)-based inverter and ring oscillator electronic circuits using the dielectrophoresis (DEP) method. The electrical property of fabricated CNTFET-based devices was measured. The CNTFET-based inverter shown electrical transfer characteristics, while the CNTFET-based ring oscillator demonstrated oscillation characteristics, denoting that the CNTFET-based circuits can function well for the application of electronic circuits. The DEP-based fabrication method is scalable, and could be used for the wafer-scale fabrication of carbon nanotube electronic circuits.

1. Introduction

Single-walled carbon nanotubes (SWCNTs) have been investigated extensively in past years for the application of nanoelectronic devices [1–5], due to their unique electrical properties such as high current-carrying capacity, high mobility, and ballistic quantum transport [6,7]. The carbon nanotubes (CNTs) with a diameter of several nanometers have a strong quantum-confinement effect in all directions perpendicular to the tube, resulting in ballistic transport in the tube for electrons and holes. These properties are not available in bulk electronic materials and can make CNT-based field-effect transistors (CNTFETs) operate much faster without energy dissipating in the tube [8].

Although there has been extensive research in the fabricating CNT-based devices such as single CNTFETs [9–15] and CNT electronic circuits [16–29], report on the wafer-scale fabrication of CNTFET-based electronic circuits is still highly interesting [30–33]. In this paper, we report the fabrication of carbon nanotube field-effect transistors (CNTFETs)-based inverter and ring oscillator electronic circuits using the dielectrophoresis (DEP) method. The inverter and ring oscillator circuits were implemented with only p-channel CNTFETs using the methodology of transistor-resistor logic [34], where a CNTFET was biased to function as a resistor. The CNTs were aligned onto the electrodes for the fabrication of CNTFET-based circuits using the electric field-directed dielectrophoresis (DEP). Dielectrophoresis (DEP) is a translational motion of neutral matter caused by polarization effects in a nonuniform electric field, and has been investigated theoretically and experimentally for deposition and alignment of CNTs recently [35–40]. Ultra-high density alignment of CNTs can be obtained with optimizing the ac frequency, the trapping time, and the CNT solution concentration in the DEP process [41,42]. Impurities in CNTs, especially the metal-containing impurity, could result in CNTFETs to be electrically shorted, and cannot be tolerated in the fabrication of electronic devices and circuits [43,44]. The DEP-based alignment and deposition of CNTs has advantage over other methods, allowing ultra purification of CNTs with filtering the impurities in CNTs using various chemicals. In addition, the DEP-based fabrication of carbon nanotube electronic circuits is compatible with the integrated circuit (IC) fabrication, and could lead to the wafer-scale fabrication of CNT electronic devices and circuits.

2. Experimental details

Ultra-purified SWCNTs (Carbon Nanotechnologies, Inc.) were used for the fabrication of CNTFET-based electronic circuits in this research. *N*-methyl pyrrolidone (NMP) was employed as the solvent for the purification and dispersion of SWCNTs, and ac dielectrophoresis (DEP) was used for the deposition and alignment of SWCNTs in the fabrication of CNTFET-based inverter and ring oscillator [45,46]. The SWCNTs were subjected to a purification process before being applied to the device fabrication. 3 mg SWCNT powder was added to 20 ml NMP and sonicated for 1 h. After being sonicated in the NMP solution, the SWCNTs have a length ranging from about 0.5 to 4 μm. The SWCNT solution was then centrifuged at 14,000 rpm for 30 min. The resultant supernatant was decanted for the sedimented carbon nanotubes, which were again

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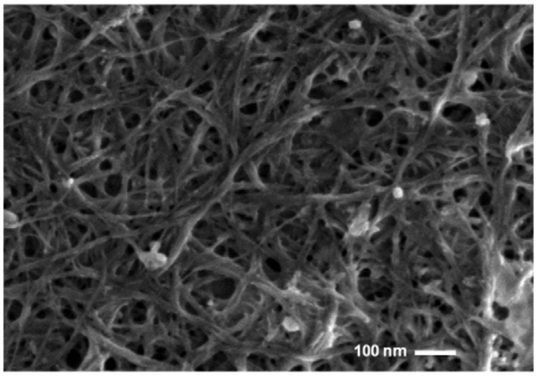

Fig. 1. SEM image of SWCNT mesh network after chemical purification and DEP-based deposition on silicon substrate.

subjected to the purification cycle with fresh NMP. Fig. 1 shows the SEM image of SWCNT mesh network after chemical purification and DEP-based deposition on silicon substrate. The prepared SWCNT–NMP solution was used in the following fabrication of devices.

Fig. 2(a) shows the schematic of a CNTFET-based inverter electronic circuit, and Fig. 3(a) shows the schematic of a three-stage CNTFET-based ring oscillator electronic circuit. Both circuits were implemented with p-channel CNTFETs only. Fig. 4 shows the schematic cross section of the CNTFET. A set of five-pieces photo masks was designed for the fabrication of the CNTFET-based inverter and ring oscillator circuits. All the CNTFETs were designed to be identical and have the same channel length (3 μm) and width (10 μm). The photo masks were fabricated by Photoscience, Inc. As the substrates, we used three-inch-diameter n-type ⟨100⟩ silicon wafers (Virginia Semiconductor, Inc.). The silicon wafers were about 350-μm-thick with a resistivity of about 3 Ω cm. The wafers initially were oxidized at 1100 °C for 20 min so to obtain a 200-nm-thick silicon dioxide layer using wet thermal-oxidation. Ultraviolet (UV) lithography and lift-off process were adopted for patterning in fabricating the devices. Shipley S1818 photo-resist was used in the UV lithography. All the thin films were deposited using electron-beam evaporation (background pressure of 2×10^{-7} Torr).

Two groups of Cr/Au electrodes including 5-nm-thick chromium (Cr) and 50-nm-thick gold (Au) were first fabricated for the deposition and alignment of SWCNTs. Dielectrophoresis was then applied to deposit and align SWCNTs across the gap of electrodes. A drop of the SWCNT–NMP solution was casted onto the electrodes, and an ac-bias with a peak-to-peak voltage of 10 V and frequency of 1 MHz was applied to the electrodes. The solvent was blown off the surface gently with nitrogen gas after 5 min. Fig. 5(a) shows the SEM image of the two groups of Cr/Au electrodes with SWCNTs aligned across the gap of the electrodes, Fig. 5(b) shows an enlarged view of a pair of electrodes

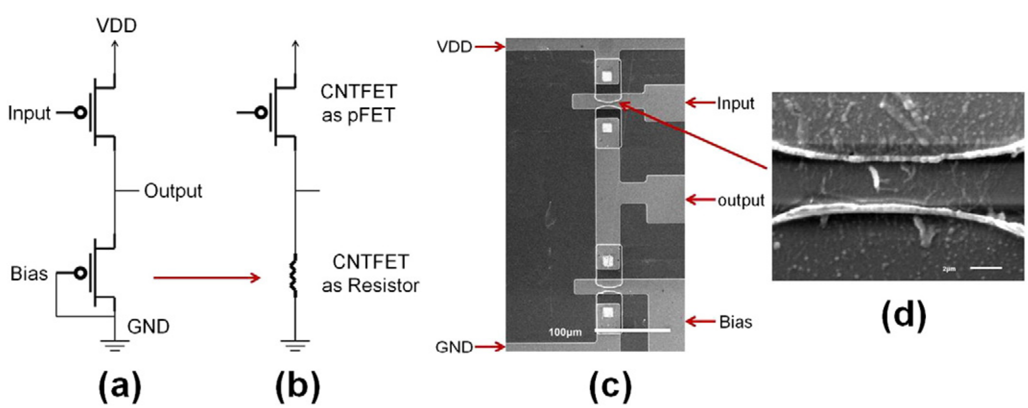

Fig. 2. (a) Schematic of a CNTFET-based inverter, which consists of two CNTFETs: the top one functions as a p-channel FET and the bottom one functions as a resistor; (b) an equivalent circuit; (c) SEM image of a fabricated CNTFET-based inverter; (d) SEM image of SWCNT mesh network connected between the electrodes.

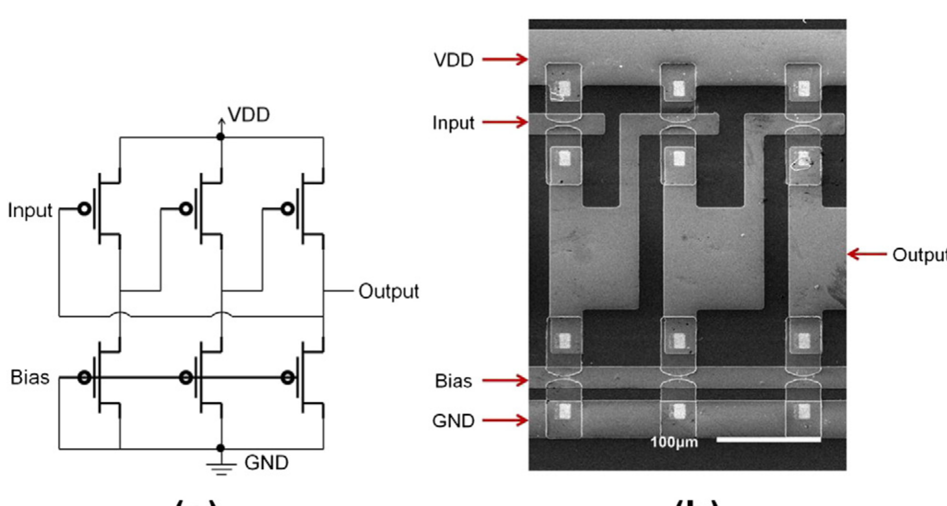

Fig. 3. (a) Schematic of a circuit consisting of three CNTFET-based inverters, where the output of the first inverter is connected to the input of the second one, and the output of the second one is connected to the input of the third one; (b) SEM image of a fabricated circuit consisting three CNTFET-based inverters, where the inverters are connected in a chain.