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Graphene-HfO2-based resistive RAM memories☆

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ABSTRACT

Graphene, a two dimensional material with remarkable electronic properties, has attracted a huge interest among scientist during the last decade. We report the fabrication of Graphene-HfO_2-based resistive RAM memories. We insert graphene layers between the oxide layer and the gold top electrode resulting in stabilization of a low resistance state stability without applied voltage, contrary to behaviour observed for identical graphene free memory devices. Graphene here is used as an oxygen reservoir and contribute to the switching mechanism.

1. Introduction

Resistive random access memory (RRAM) based on Metal-Insulator-Metal structure is a promising candidate for next generation of non-volatile memory [1] beyond the 22 nm node as regards of its simple scalability, high speed operation and low operation voltage [2–5].

The RRAM device operation is based on resistance switching between two bi-stable resistance states: an initial high resistance state also named OFF state and a low resistance state (ON state). The OFF-to-ON transition is designed as "Set" operation and is triggered by voltage biasing. The reverse ON-to-OFF transition ("Reset") can be observed by applying either a voltage of the same polarity as the Set stage ("unipolar" device) or a voltage of the opposite polarity ("bipolar" device).

The formation of a single or multiple conductive channels consisted of oxygen vacancies between the two electrodes is the largest promoted model for HfO_2-based resistive RAM devices [6–8]. Various mechanisms have been proposed for the oxygen vacancies creation such as hot electron impacts or redox reactions [9–11]. The resistance recovery during reset operation was attributed to oxygen ions back diffusion and their recombination with oxygen vacancies leading to the conductive channels rupture [12,13]. Following this model a source of oxygen ions is needed for reset operations.

Different techniques were proposed to support oxygen storage: doping cluster into the oxide [14,15], interfacial layer (Ti ad layer) as oxygen buffer [16,17], direct oxygen reservoir effect supported by the anode which allows storage of extracted oxygen ions during Set operation [18,19]. or porous electrodes which permit oxygen circulation between the oxide and the ambient atmosphere [20].

2. Graphene based OxRAM

In this work, we investigated the use graphene as interface layer between hafnium oxide and a metallic top electrode used as anode for enhance oxygen reservoir effect. The literature reports studies of coupling graphene and hafnium oxide but were mainly focused on MOS applications: determination of graphene electron mobility [21,22]. or dielectric deposition and conformity on graphene [23,24]. Utilization of graphene based materials for resistance switching memories is still few documented, even if resistance switching in graphene oxide was reported [25,26]. Use of graphene as active electrodes for RRAM devices were presented but was mainly focused on graphene used as a bottom electrode for flexible electronic compatibility [27,28] due to its ability to be bent without disruption. However the impact and modification brought by the use of graphene on electrical resistance switching properties is still unidentified. Nevertheless, in a recent study [29], graphene was used in TiO_2 based RRAM and put in evidence incidence on switching properties leading to the transition from unipolar to bipolar devices. However the effect was not related to oxygen migration and

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didn't clearly put in evidence oxygen reservoir effect of graphene mentioned above. More recently, the use of a graphene adlayer at the anode in Pt/HfO_2/TiN memory stacks was reported [30]. Improvements of pre-existing memory properties were underlined.

Here we report an original structure leading to graphene intercalation in the Metal-Insulator-Metal device. Graphene is on top of the HfO_2 thin oxide and the metal contacts are deposited directly on the graphene layers. Due to its lack of oxidation, gold is not suitable as a top electrode for HfO_2 based resistive memories. A thin layer of graphene intercalated in-between the oxide and the gold top electrode is sufficient to obtain the memory effect in the device.

3. Experimental setup and device fabrication

We first deposit a 10 nm seed layer of TiN by Physical Vapour Deposition (PVD) at 350 °C on a p-type silicon wafer (100) and the deposition of platinum was made by Atomic Layer Deposition (ALD). The deposition was made at 250 °C and the platinum thickness is about 25 nm. The thin oxide layer is also deposited by ALD and consists of 10 nm of the high-k dielectric material HfO_2. The deposition was made at 350 °C with 99 ALD cycles.

Graphene was synthesized on 8 in. p-type silicon wafer (100) with a Ni/a:SiCH/SiO_2/Si multi-stack annealed at 700 °C during 3 min. The carbon from the amorphous silicon carbide layer is driven through the nickel layer thanks to its low solubility when heated. After annealing, multilayer graphene appears on top of the nickel [31].

After the graphene growth on nickel, the carbon material has to be transferred on the HfO_2/Pt/TiN/Si base substrate. A thin layer of PMMA (800 nm) is spin coated on the Graphene/Ni/a:SiCH/SiO_2/Si wafer and dipped in 27% $FeCl_3$ solution to remove nickel. After few hours when all the nickel is etched, the Graphene/PMMA layer is floating in the acid-bath and is then rinsed several times in deionised water. This layer is then fished from beneath with the HfO_2/Pt/TiN/Si based substrate. After annealing the resulting sample at 180 °C and removing the PMMA in acetone, the graphene is standing directly on HfO_2.

The gold top electrode was deposited by evaporation through a solid grid with aperture of 2 mm diameter, used as a shadow mask. The thickness of the gold electrode is evaluated to be included in the 30–50 nm range. It results in an array of gold round electrodes on top of the graphene.

This metal electrode is used as a hard mask to etch graphene between the circular devices. Oxygen plasma (600 W) is then applied during 5 min to remove the graphene and to prevent from short-circuiting devices.

Fig. 1 shows the final device structure: a multi-stack of top-electrode-Au/Graphene/HfO_2/Pt/TiN/Si. The top electrode has a diameter of 2 mm.

Electrical characterizations were performed in air with a Keithley 2635 Source Meter unit. The Pt bottom electrode was electrically grounded. All voltages are applied to the gold top electrode and will be referred to it.

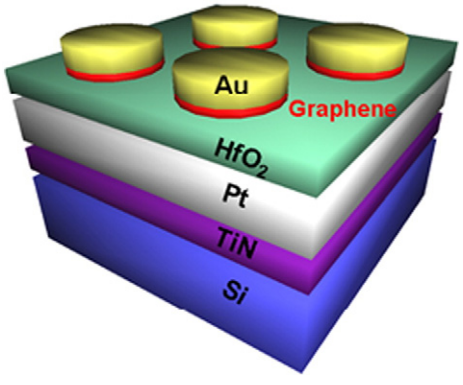

Fig. 1. Metal-Insulator-Metal structure for Resistive RAM: Au/Graphene/HfO_2/Pt/TiN/Si stack. Top electrode diameter is 2 mm.

Fig. 2a shows a Scanning Electron Microscopy image of the graphene material on nickel. The inset is a high resolution image showing the graphene wrinkles that are attributed to the difference in the thermal expansion coefficients of graphene and Ni, which induces a thermal stress during the cooling. Fig. 2b displays the Raman spectrum of the corresponding sample transferred on 300 nm SiO_2. It shows clearly the presence of graphene thanks to the appearance of characteristic 2D peaks at 2722 cm^{-1}. This spectrum exhibits also a G peak at 1583 cm^{-1} and a small D peak at 1361 cm^{-1} with an I_D/I_G ratio of 0.08 indicating a relative low defect density probably originating from few sp^3 carbon atoms or defects. I_{2D}/I_G ratio is equal to 0.52 and a 2D full width half maximum of ~63 cm^{-1} is estimating the growth of 7–15 layers of graphene.

This number of layer is an estimation [32] and is correlated by the TEM pictures. (Fig. 2c and d).

A dual focused ion beam – scanning electron microscope (FIB-SEM, FEI Helios 450S) is used to prepare the thin lamella for transmission electron microscopy (TEM) characterizations. The lamella is thinned until a thickness of about 50 nm, and then characterized by TEM (FEI Tecnaï, 200 keV) on transversal cross-section. It must be noted that each sample was coated with an e-beam induced Pt deposit in order to protect the Metal-Insulator-Metal stacking prior to the milling.

TEM characterizations on the thin lamella (Fig. 2c) shows the complete MIM stacking used for the device: Au/Graphene/HfO_2/Pt/TiN/a small SiO_2 interface layer/Si. A HRTEM image (Fig. 2d) clearly puts in evidence that a multilayer graphene of about 6 nm (15–18 layers) has been intercalated between the dielectric and the top electrode in gold. (The thickness of the graphene layers varies from 1 to 20 nm overall the sample and hence each gold top electrode has different number of graphene layers underneath).

4. Electrical characterizations

Electrical characterizations of resistive switching properties of the samples without graphene adlayer between hafnium oxide and gold top electrode are performed using Current-Voltage (I-V) measurements. Previous studies [33] on these stacks have shown typical bipolar resistive switching: the applied voltage for set and reset operations have opposite polarities. Positive voltage sweeps from 0 V to 8 V to 0 V are applied on the top electrode to assess the set operation and ON state resistance retention. A current compliance is fixed at 10^{-4} A to prevent irreversible electrical breakdown of the dielectric during Set operation. Reset operations are triggered by the application of an opposite polarity voltage sweep, current compliance in this case is increased to avoid limitation of the applied voltage by the feedback loop of the compliance.

Fig. 3 a presents I-V curves obtained for HfO_2/Pt graphene-free sample with evaporated gold top electrode. When the applied voltage stays below 4 V, the sample remains in an insulating state which define the OFF resistance state. The low value of current near 10^{-9} A observed is in good agreement with precedent investigations. At $V = 4$ V, Set operation begins: the current abruptly increases and reaches the compliance value. For voltages above the Vset, a high conduction state is established: the sample has reached the ON state resistance. When the voltage sweep returns progressively to zero, no retention of the ON state occurs, there is no memory effect. Repetitions of positive voltage sweeps always provide the same result. Several values for current compliance from 10^{-6} A up to 10^{-3} A have been tested to exclude an effect of this limit. An unstable ON state is always observed for this stack configuration. The following negative voltage swept confirms the absence of retention. The exhibited current is in the same order of magnitude as noticed in the initial OFF state: 10^{-8} A. The origin of this phenomenon will be discussed later.

The representative I-V characteristics for graphene-gold electrodes are represented in Fig. 3b. Alternatives positives and negatives voltage