



Research paper

Positive-bevel edge termination for SiC reversely switched dynistor[☆]Lin Liang^{*}, Ming Pan, Ludan Zhang, Yuxiong Shu

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ABSTRACT

The termination structure for the pulsed power switch SiC RSD (reversely switched dynistor) is studied in this paper. According to the structure characteristics of SiC RSD, the positive-bevel edge termination is designed. By establishing the two-dimensional numerical model, the function that the positive-bevel can reduce the surface electric field is proved. Combined the surface electric field and the area loss, 45° positive angle is selected. According to the process characteristics of SiC material, bevel dicing together with ICP (inductively coupled plasma) etching treatment is chosen to fabricate the positive-bevel edge termination in experiment. The forward blocking voltage of about 600 V is acquired for the device. The optimal value for the etching depth is also discussed.

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1. Introduction

RSD (reversely switched dynistor) was proposed in the 1980s by the Russian scientist Prof. I V Grekhov as a special type of device applied in pulsed power area [1]. The outstanding characteristics of RSD are the low dissipation, high di/dt capability and good voltage-sharing in series. After about 30 years' development, Si-based RSD has nearly reached the limit of Si material [2–6]. As the next generation wide bandgap semiconductor material, SiC has the advantage of twice carrier saturation drift rate, three times of thermal conductivity, three times of bandgap and ten times of dielectric breakdown field of Si. Therefore, it is considered as an ideal choice for power device fabrication [7–8]. With the development of the high-quality epitaxial wafers and process technology, the SiC bipolar devices have become practical. We proposed the RSD device based on 4H-SiC for the first time, and established a two-dimensional numerical model to argue the feasibility of its operation principle [9]. It will bring higher monolithic blocking voltage and better repetitive frequency performance to make the RSD by SiC material.

RSD is a kind of two-electrode device whose forward conduction is triggered by reverse pre-charge. It doesn't have the reverse blocking capability, and blocks high voltage in forward direction at off-state. Though SiC material has the dielectric breakdown field of about 3 MV/cm, which can make us get high blocking voltage by thin chip, it is still

a theoretical value. The voltage rate of the practical device is more dependent on the design and process of the junction termination. The main target of the junction termination design is to extend the spread of the electric field line at surface, so as to reduce the surface electric field and enhance the breakdown voltage. There are planar type and mesa type for the common termination structures, including field plate (FP), field limiting ring (FLR), junction termination extension (JTE), variation of lateral doping (VLD), bevel edge termination and so on [10–13]. Because the blocking junction of the forward voltage for RSD is a deep junction from the upper surface view, and the space charge region extends upward in the drift layer, the planar termination is not suitable here. We choose the positive-bevel edge termination structure.

The mesa termination has been developed early in the Si-based high voltage devices, such as diode, thyristor, etc. The analysis show that the positive-bevel (junction area decreases from high concentration side to low concentration side) can reduce the surface electric field, while the negative-bevel (junction area increases from high concentration side to low concentration side) can do that with a small enough angle. For the Si-based power devices, the bevel is formed by blasting sand and grinding angle, together with etching, or by trenching of wet etching with special recipe. For the SiC-based devices, wet etching is not feasible. Dry etching is a kind of way, but it is not easy to control to form such kind of deep and angle required trench in practice. The blasting sand and grinding angle way don't work, for SiC material has high hardness. X. Huang et al. have reported the bevel edge termination formed by sawing the SiC wafer with a V-shaped dicing blade [13], which could be seen as an effective way for the SiC mesa termination fabrication. This process is applied in the SiC RSD of four layer structure in this paper. The function of reducing the surface electric field by the positive-bevel is analyzed quantitatively by the simulation model firstly,

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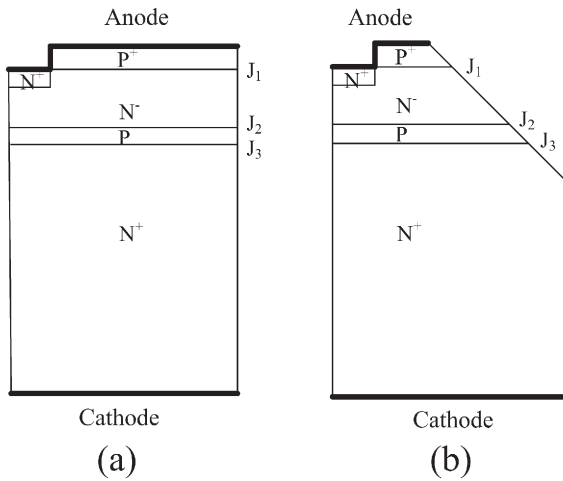


Fig. 1. SiC RSD cell structure. (a) Without positive-bevel edge termination. (b) With positive-bevel edge termination.

then 45° angle is selected to be carried out in process, and the influence on the blocking characteristics of the etching treatment after the V-shaped dicing is discussed.

2. Simulations and calculations

Fig. 1 shows the cell structure of the SiC-based RSD. RSD is a two-electrode four-layer thyristor-type device. It consists of several thousands of alternating P⁺N⁻PN⁺ thyristor and N⁺N⁻PN⁺ transistor sections. The forward voltage is blocked by the central J₂ junction (collector junction common to all units). A short reverse voltage is applied to the device at triggering, with the avalanche breakdown of the J₃ junction at cathode [9]. Fig. 1(b) shows the cell structure with positive-bevel edge termination. Generally speaking, the positive bevel refers to J₂. As could be seen, the junction area decreases from P-base side to N-base side. It is worth of pointing out that this bevel will go through all of the three junctions J₁, J₂ and J₃ in the device. It is also a positive-bevel for J₃, which will benefit the triggering process.

In order to analyze the function that the bevel edge termination reduces the surface electric field, the two-dimensional numerical model for SiC RSD with the bevel edge termination is established. The device structure is just set as shown in Fig. 1(b). The width of the N-drift region is 12 μm and the concentration is 8 × 10¹⁵ cm⁻³. The mobility model, the Shockley–Read–Hall recombination model, the Auger

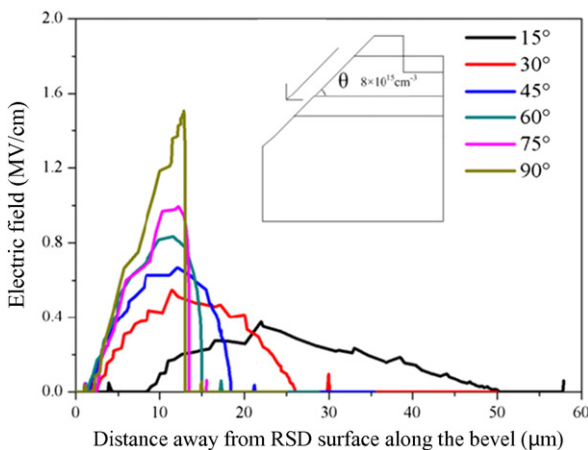


Fig. 2. Electric field distribution along the bevel surface with the angle of 15°, 30°, 45°, 60°, 75° and 90°.

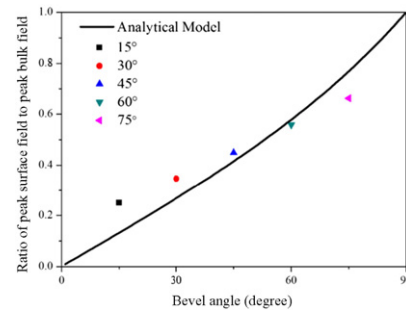


Fig. 3. Electric field simulation comparison between analytical and numerical models.

recombination model, the impact ionization effect and the bandgap narrowing effect are used. The parameters for the carrier mobility and lifetime are set separately for different regions considering doping concentration. In the forward blocking mode, the surface electric field distribution on the positive bevel is calculated based on the SiC RSD model. The surface of the P⁺ region at anode is set to be the original point and the distance along the bevel is set to be the lateral axis. With the ideal forward breakdown voltage of 770 V, when the positive bevel angles are 15°, 30°, 45°, 60°, 75° and 90°, the surface electric field along the bevel is shown in Fig. 2. The electric field mainly distributes on the N⁻ drift layer. It is the bulk electric field for the 90°. Thus it could be seen that the smaller the angle is, the lower the surface electric field is, which agrees with the analytical model of the positive-bevel edge termination [12]. The peak electric field for the numerical model and the analytical model is compared in Fig. 3, and the simulated results agree basically. The main cause for the error is related with the weak forward biased junctions J₁ and J₃ at forward blocking in the four layer structure of RSD. When the positive bevel angles are 15°, 30°, 45°, 60° and 75°, the ratios of peak surface field to peak bulk field are 25.0%, 34.7%, 44.9%, 55.9% and 66.3%, respectively, for the numerical model.

Though the surface electric field decreases with the positive angle reduced, the loss for the effective chip area increases. Fig. 4 shows this tradeoff relationship, where the SiC wafer dimension is 5.4 mm × 5.4 mm. Combined the electric field reduction and the area loss, we have chosen 45° bevel in the experiment.

3. Experiments

The epitaxial wafers in the experiment come from Cree Inc. The three epitaxial layers of P-type, N-type and P-type are grown successively on the N⁺ substrate, the width of which is 350 μm. The concentration and width of each layer are set to be the same as the parameters of the simulated model. After the lithography, the selective ICP

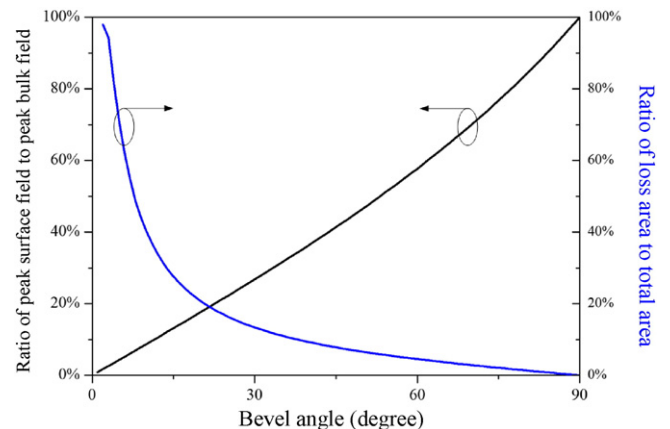


Fig. 4. Tradeoff between electric field reduction and area loss.

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