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# Interface state density dependence on detection process in single electron photo-detector (photo-SET)

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ABSTRACT

In this paper, we report the effect of optical power on interface state density ($D_{it}$) for the ultrasensitive single electron photodetector (photo-SET). To perform this work, Conductance–Capacitance–Voltage ($C$–$G$–$V$) techniques have been used, which form a method for the characterization of interface traps in MIS structures, taking into account the effect of the series resistance ($R_s$) at room temperature. To calculate the value of the density of interface states, ($C$–$G$–$V$) sweeps need to be corrected, analyzed and all extracted parameters would need to be recorded. Using Hill-Coleman method and a program developed using MATLAB, the calculated value of these interface state density ($D_{it}$) at 1 MHz was $2.4 \cdot 10^{12}$ $eV^{-1}$ $cm^{-2}$.The value of the interface state density ($D_{it}$) increase with increasing optical power.

## 1. Introduction

Several years ago, nano-technology enabled us to fabricate very small structures with capacitance small enough to observe the charging effects of discrete electrons. When the charging energy $e^2/2C$ of the island with capacitance C becomes larger than the energy $K_BT$ of the thermal fluctuations, the entrance of one electron results in a noticeable recharging of the island capacitance, so that electron transfer is strongly suppressed. Based on this coulomb blockade effect, several devices have been proposed and demonstrated [1,2]. One of the first successful devices to be based on this effect was the single electron transistor (SET) developed by Fulton and Dolan [3]. Since its inception in the optoelectronics and communication industries, (photo-SET) have been extensively studied and researched both at the academic and industrial levels, the characterization of these device requires analysis of their interface states. Various experimental techniques via conductance technique of Goetzberger and Nicollian (1967), quasistatic technique of Kuhn (I970), Castagne (1968) and Castagne and Vapaille (1971) for measuring the density of interface states and their behavior are available in literature. In (1980), a simpler and quick conductance approximation technique has been proposed and used by Hill and Coleman which we use in our work to determine the interface state density.

In this paper we report a detailed analysis of single photo-generated traps situated inside the gate oxide of (photo-SET). The interface state density ($D_{it}$) has been analyzed by $C$–$G$–$V$ measurements using Hill-Coleman method. The presence of slow traps situated at the interface ($Si/SiO_{x\,=\,1.5}$) was evidenced [4]. These traps are influenced by optical power excitation. Numerical simulations have been used in order to determine (Series resistance ($R_s$), oxide capacitance ($C_{ox}$), corrected conductance ($G_C$), corrected capacitance ($C_C$). These parameters are used to determine the density of interface states using Hill-Coleman method.

## 2. Experimental details

The single electron photodetector (photo-SET), or nanopixel was developed in the Sherbrooke University combining nanolithography and reactive ion etching (RIE) process. The schematic cross-sectional structure of nanopixel device discussed in this paper, is shown in Fig. 1(a). We report the fabrication and insulation of nanopillars, in which a layer of silicon rich oxide (SRO) deposited by low–pressure chemical-vapor deposition (LPCVD) is present between two layers of highly doped polysilicon. The NCs are formed by annealing the SRO in nitrogen environment. After the annealing, Si dots appear in thick and thin layers. The oxide is composed of silicon NCs (Si-NCs) embedded in $SiO_{x\,=\,1.5}$ layer. The thick $SiO_{x\,=\,1.5}$ layer presents spherical Si crystallites with an average size; around 5 nm extracted from transmission electron microscopy (TEM) measurements. A second annealing step in oxygen was also performed. We used e-beam lithography and dry etching to obtain the vertical structures. These nanopillars are fabricated with diameters of 2 μm, 500 nm, 200 nm and 100 nm. Fig. 1(b) shows the scanning electron microscopy (SEM) image of nanopillar. The electrical insulation is provided by planar photosensitive resistance; it was spun and then etched back by $O_2$ plasma. Then chromium/gold electrodes are made by lift-off on the top of the columns. The substrate is used for electrical

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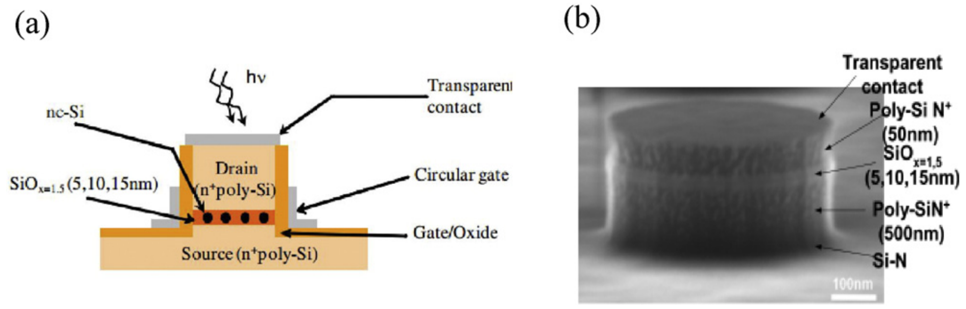

**Fig. 1.** (a) The schematic stack of a nanopixel (photo-SET) and (b) SEM micrograph of the studied nanopixel.

continuity. The (*C*–*G*–*V*) measurements were performed using a HP4194 machine at room temperature.

## 3. Results and discussions

### 3.1. I(*V*) measurements

I(V) characteristics were recorded in the dark and under optical excitation. Fig. 2 shows that the photo-SET is sensitive to light.

The absorption of visible light provide to electrons an energy $E_{ph} \approx h\upsilon$. We consider here the photon energy greater than the band gap of silicon. When photons reach the ZCE, they are absorbed by the silicon. Then there are creations of electron/hole pairs, which are separated because of the electronic field that reigns at this location.

## 4. *C*–*G*–*V* measurements under dark conditions

The voltage dependent capacitance and the conductance of the device can be used to calculate interface properties. Various techniques have been used to achieve this. One of the techniques is conductance technique, which determines the point-to-point density of states throughout the depletion region of such devices [5]. The conductance technique determines the surface parameters with more accuracy than capacitance technique [6], because the conductance comes only from the interface states [5]. The conductance losses are the base of conductance technique, resulting from the exchange of majority carriers between the interface states, when a small AC signal is applied to the devices [7].

Fig. 3 shows the measured capacitance (*C*) and measured conductance (*G*) of Si/$SiO_{x\,=\,1.5}$.
structure as a function of voltage. We observed a significant peak at −4.5 V. This is probably due to interface traps [8,9].

The series resistance of the device can cause errors in the extraction of interface properties in a MIS structure. In order to get accurate results, the *C*–*V* and *G*–*V* data sets must be corrected of this series resistance ($R_S$). The real series resistance of the structure can be determined from the measured capacitance and conductance in strong accumulation region [10,7]. The series resistance, when the MIS structure is in strong accumulation region, can be represented as [7]:

$$R_S = \frac{G_{ma}}{G^2{}_{ma} + w^2 C^2{}_{ma}} \tag{1}$$

where $G_{ma}$ and $C_{ma}$ are measured conductance and capacitance in strong accumulation region, respectively. The capacitance of insulator oxide layer ($C_{ox}$) is related to series resistance given by [7]:

$$C_{ma} = \frac{C_{ox}}{1 + w^2 {R_s}^2 C^2{}_{ox}}. \tag{2}$$

From Eqs. (1) and (2), $C_{ox}$ can be written as

$$C_{ox} = C_{ma}\left[1 + \left(\frac{G_{ma}}{wC_{ma}}\right)^2\right]. \tag{3}$$

The corrected capacitance ($C_c$), and corrected equivalent parallel conductance ($G_c$) for series resistance, are obtained as a function of angular frequency from the measured capacitance and conductance by [7]:

$$C_c = \frac{\left({G_m}^2 + w^2 {C_m}^2\right) C_m}{a^2 + w^2 {C_m}^2} \tag{4}$$

$$G_c = \frac{\left({G_m}^2 + w^2 {C_m}^2\right) a}{a^2 + w^2 {C_m}^2} \tag{5}$$

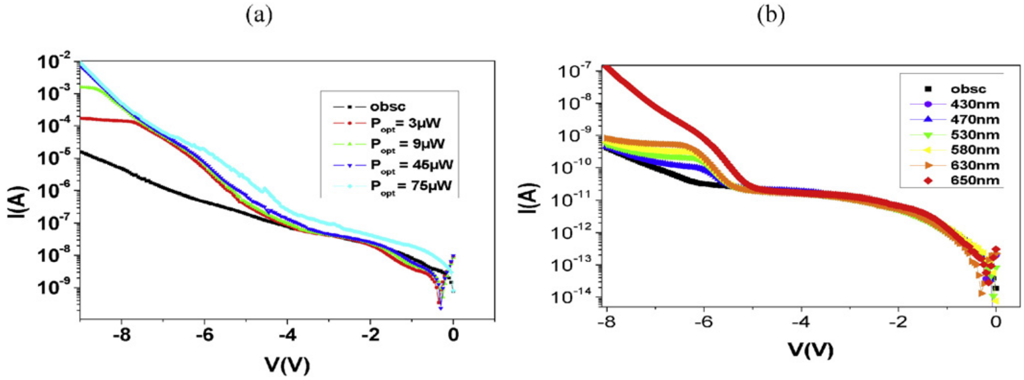

**Fig. 2.** I(V) measurement for various (a) optical powers and (b) and the wavelengths of the visible.