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Copper electroplating technique for efficient manufacturing of low-cost silicon interposers

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ABSTRACT

Through-silicon via (TSV) technology is the heart of 3D integration technology. An approach was proposed to simplify the integrated process flows. Dry film photoresist was introduced in the through via filling process. Cu-TSVs and Cu-pads were formed simultaneously through the electroplating process, which diminished the interface between Cu-TSVs and Cu-pads. This approach simplified the integrated process flows, enhanced the reliability, and lowered the costs dramatically compared with the most preferred TSV fabrication method in the industry today, which would have a broad application in the 3D integration industry.

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1. Introduction

High-speed, multi-functional, and small electronic devices have been enabled by the high integration technologies, which comes to reality through the miniaturization of the large-scale integration (LSI) process scaling.[1] However, the miniaturization will be limited because of the increase of leak current which generates heat in transistors and signal delay caused by the wiring [1,2]. 3D packaging technology is one of the technologies that enables high density integration that does not depend on miniaturization on 2D surface [1,3]. Through-silicon via packaging technology (TSV technology) is the heart of 3D integration technology, which provides a number of significant advantages, such as high performance, low energy consumption, and the small form factor [4].

Depending on the application, there are two kinds of approaches for the vertical integration through the TSV technology: via first and via last [5]. In the via first method, similar to the Damascene application, vias are filled from the front side of the silicon wafer. Then the wafer is thinned to expose the TSV electrodes. While in the via last method, the via filling is conducted after the wafer is thinned [5]. Due to the difficulties in handling and plating thin wafers, the via first approach becomes the most preferred TSV stacking method in the industry at present. Both via first and via last approaches, they all approximately contain the following steps: (i) via etching on the wafer, (ii) insulator deposition, (iii) barrier and seed layer deposition, (iv) via filling, (v) surface copper removal through chemical mechanical polishing (CMP), (vi) support wafer bonding, (vii) wafer thinning, (viii) pad electroplating, and (ix) wafer/chip alignment, bonding and dicing [3, 5]. These approaches are complex. There exists strain distribution in surrounding silicon induced by the three-dimensional Cu-filled through-silicon via features [6–11]. The interface between the Cu pillar and the pad may affect the strain distribution and the electrical/mechanical properties of the silicon interposer. It is reported that the through vias are sputtered using copper and electroplated on both via sidewall and wafer surface [12–16].

In this paper, a simplified approach is proposed to manufacture the silicon interposer. First, the through vias are etched on the wafer. Second, dry film photoresists are pasted on both sides of the wafer. Third, the dry film photoresists in the pad areas are removed, and then electroplating is conducted. The copper pads are formed on both sides of the Cu-TSV pillar during via filling process, which may simplify the three-dimensional integrated process flows and lower the process costs significantly.

2. Material and methods

The electrolyte used for TSVs filling consists of 80 g/L Cu^{2+} ($Cu(CH_3SO_3)_2$), 20 g/L CH_3SO_3H, and 50 mg/L Cl^-. Three kinds of commercial additives including accelerator, suppressor and leveler are used in the experiment. Two phosphorus-containing copper slices are used as anode. First, through vias (Ø 50 μm × 200 μm) are prepared using deep reactive ion etching (DRIE) technique in a 3-inch silicon wafer (thickness: 200 μm), and then a thermal-oxide layer, Ti adhesion layer (ca. 40 nm) and Cu seed layer (ca. 1500 nm) are manufactured,

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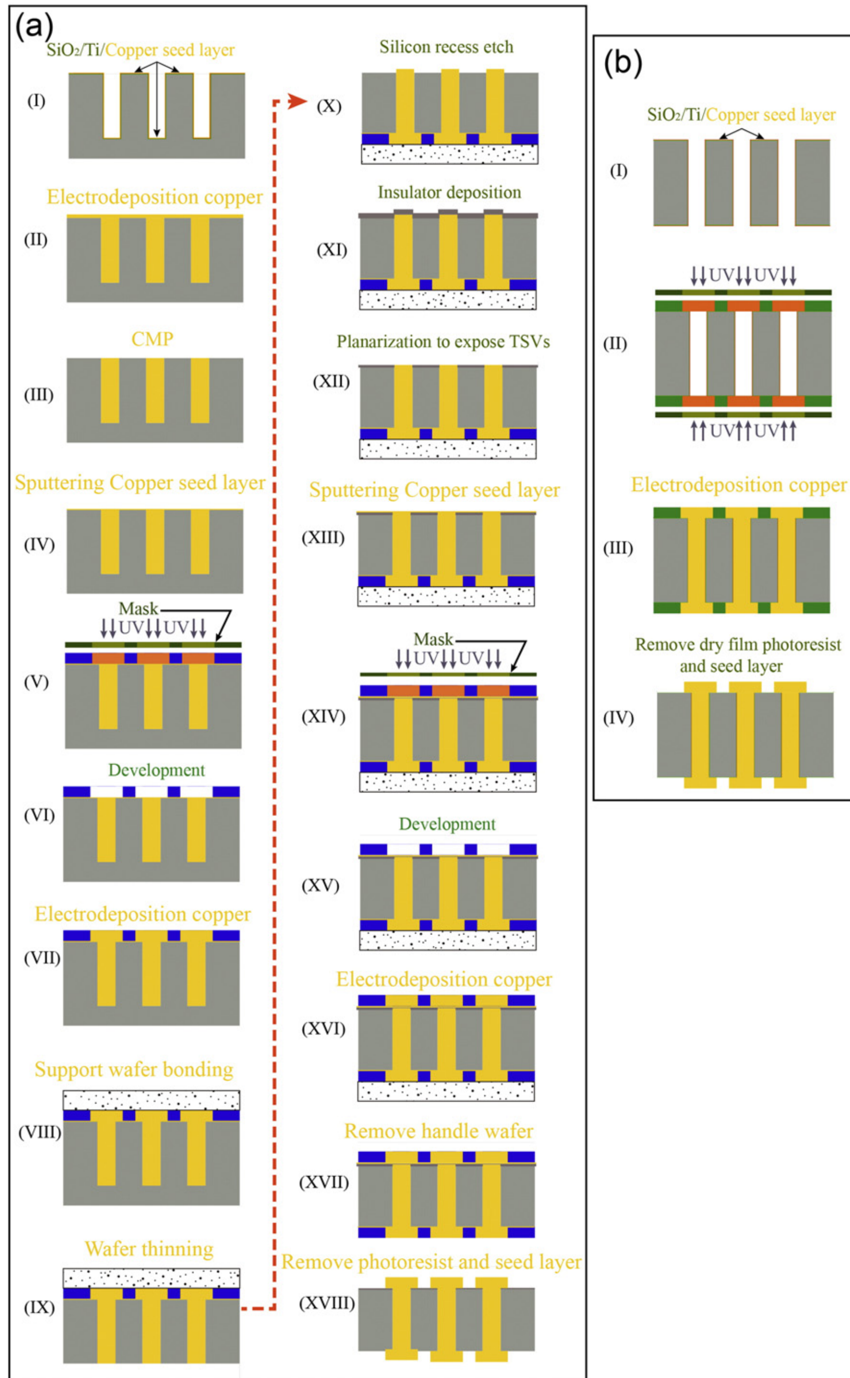

Fig. 1. Schematic of the process flows of TSV fabrication for 3D IC integration. (a) Blind via filling and pad fabrication, (b) Through via filling and pad fabrication proposed in this paper.

sequentially. Second, the dry film photoresists are pasted on both sides of the wafer through the hot pressing technique. The basic process comprises the following steps: (a) The heating roller is heated up to 100 °C, (b) As shown in Fig. 2, the dry film resist is laminated at 100 °C with an appropriate pressure using a laminator to paste it onto one side of the wafer, and the other side of the wafer is pasted by the dry film resist using the same method, (c) The mylar sheets are removed. Third, the dry film photoresists in the pad areas (diameter: ca. 100 μm) are removed through the exposure and development processes. At last, the electroplating is conducted in a temperature-controllable cell (ca. 27 °C) with a current density of 8 mA/cm^2. As shown in Fig. 4, each side of the wafer is placed one phosphorus-containing copper slice as anode. The cross-sectional images of Cu-TSVs with pads are achieved

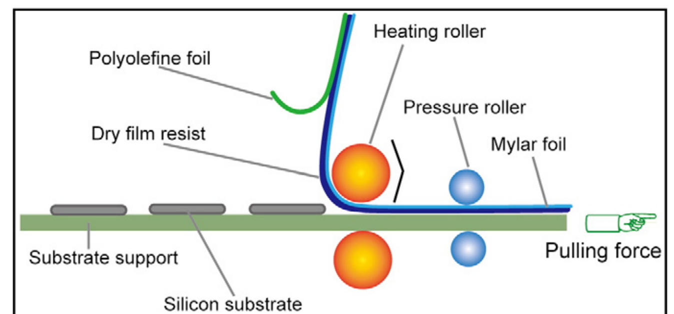

Fig. 2. Overview of the adhesive bonding process between dry film photoresist and silicon wafer by lamination.

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