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Effects of single grain boundary and random interface traps on electrical variations of sub-30 nm polysilicon nanowire structures

Hyeongwan Oh [a], Jungsik Kim [b], Junyoung Lee [a], Taiuk Rim [c], Chang-Ki Baek [c], Jeong-Soo Lee [a,*]

[a] Department of Electrical Engineering, Pohang University of Science and Technology (POSTECH), Pohang 790-784, Republic of Korea
[b] Division of IT Convergence Engineering, Pohang University of Science and Technology (POSTECH), Pohang 790-784, Republic of Korea
[c] Department of Creative IT Engineering and Future IT Innovation Lab., Pohang University of Science and Technology (POSTECH), Pohang 790-784, Republic of Korea

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ABSTRACT

Effects of single grain boundary (SGB) and random interface traps (RITs) on the electrical characteristics of the macaroni structure in sub-30 nm poly-silicon (poly-Si) channel devices are analyzed using 3D simulation. The macaroni structure can mitigate the adverse effects of SGB on the electrical variations compared to the conventional structure. However, when RITs are considered at the interface between the dielectric filler and the poly-Si channel, the macaroni structures show relatively larger variations due to RITs at the inherent interface, compared with the conventional devices. Thus the reduction of interface traps in the macaroni devices is critical for sub-30 nm poly-Si device applications.

1. Introduction

Three-dimensional (3D) stackable architectures are considered as a promising solution in order to overcome the scaling limitations of planar devices [1–4]. Most of 3D structures adopt poly-crystal silicon (poly-Si) channel because of the difficulties of crystalline channel process and low fabrication cost [5–10]. However, the grain boundary (GB) in the scaled poly-Si channel can cause the electrical fluctuations in the threshold voltage (V_{th}), the subthreshold swing (SS), and the drain current [11,12]. In order to overcome the GB problems in poly-Si, the macaroni structure with the silicon-oxide (SiO_2) dielectric filler (DF) inside the channel has been proposed [13]. The superior immunity from the electrical variation by reducing the number of GB traps in the channel and an excellent subthreshold swing behavior has been demonstrated [13,14]. The vertical macaroni Field Effect Transistors (FETs) were applied in the Bit-Cost Scalable (BiCS) and showed that the SS decrease and the on-current increase by thinning Si thickness of the macaroni FETs [1516]. The macaroni channel structures have been adapted in other 3D stackable device candidates such as Stacked Memory Array Transistor (SMArT) and Terabit Cell Array Transistor (TCAT) where they showed excellent V_{th} distribution and electrical characteristics due to thin body effect in the macaroni structure [17,18]. The DF diameter and the GB trap density are critical parameters where they can mainly determine the overall electrical performances in the macaroni structure. In sub-30 nm regimes, one can expect that the influence of interface traps between the poly-Si channel and the DF becomes more significant and can severely cause the electrical fluctuations [19].

In this work, the electrical variations of the scaled macaroni structures with single grain boundary (SGB) and random interface traps (RITs) are investigated and compared to the conventional structures down to 20 nm channel thickness. The macaroni poly-Si devices show less V_{th} and SS variations with the SGB only in 30 nm channel thickness. On the other hand, in sub-30 nm channel regime, the macaroni device is vulnerable to RITs compared with the conventional devices.

2. Simulation method

Using 3D simulator Sentaurus TCAD (Synopsys, Inc) [20], the effect of SGB and RITs in a macaroni structure on the electrical variation is investigated. The density-gradient model is included in the simulation to consider quantum effect [20]. Various dielectric filler diameters (D_{DF}) and channel diameters (D_{NW}) are used in the simulation in order to analyze the electrical variations in terms of V_{th} and SS.

Fig. 1 shows a cross-sectional of the 3D Nanowire FET schematic with the macaroni structure with SGB and RITs in the channel. The D_{NW} of the macaroni structure is fixed at 30 nm and the D_{DF} is in the range of 10–20 nm. The D_{NW} of the conventional structures are 30 and 20 nm, respectively. Detail simulation parameters are summarized in Table 1.

The SGB is assumed to be placed perpendicularly in the middle of the channel. The grain boundary trap state (N_{GB}) showed different energy profiles according to various post-treatment methods [21]. In our simulation, U-shaped distribution from 10^{12}–10^{14} cm^{-2} eV^{-1} is used for N_{GB} which is a typical value from the poly-Si channel without any post-treatment [22]. The RITs are randomly located at the poly-Si channel/gate oxide and the poly-Si channel/DF interface. In order to further investigate the effect of interface traps, the interface trap states (N_{IT})

* Corresponding author.
E-mail address: ljs6951@postech.ac.kr (J.-S. Lee).

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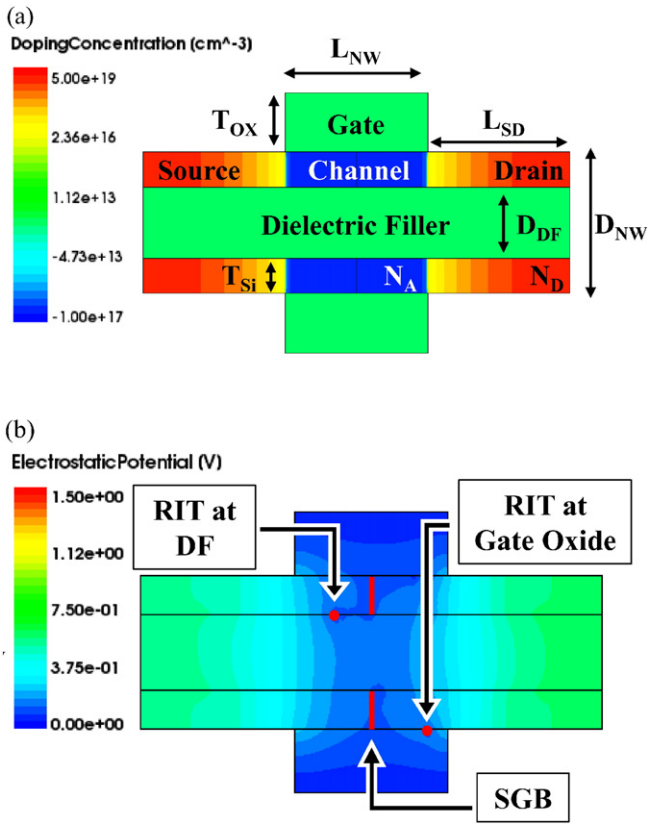

Fig. 1. A representative macaroni channel structure: a cross-sectional (a) schematic and (b) electrostatic potential profile with single grain boundary (SGB) and two random interface traps (RITs). The SGB is placed in the middle of the channel and one RIT is located at the poly-Si/dielectric filler interface and the other is located at poly-Si/gate oxide interface.

with three different values (1×10^{11}, 3×10^{11}, and 5×10^{11} $cm^{-2}\,eV^{-1}$) are used in this simulation where these values have been typically obtained in nano-scale devices using the charge pumping method [23]. The V_{th} is extracted at the constant drain current level of $I_D = 10^{-7}$ W/L (A).

3. Results and discussion

Fig. 2 shows the V_{th} and SS change with various channels and DF diameters both in macaroni and conventional devices without SGB and RITs in the channel. At the same $D_{NW} = 30$ nm, as the D_{DF} increases, the macaroni structures shows higher V_{th} and lower SS compared to the conventional structure. The macaroni with $D_{DF} = 20$ nm shows almost similar V_{th} and SS values to the conventional with $D_{NW} = 20$ nm, which has been attributed to the enhanced gate controllability with the thinner channel thickness in the macaroni structures [13,14].

Table 1
Simulation parameters.

Parameter	Description	Value
L_{NW}	Channel length (nm)	30
L_{SD}	S/D length (nm)	30
D_{NW}	Channel diameter (nm)	20, 30, 40
D_{DF}	Dielectric filler diameter [in $D_{NW} = 30$ nm] (nm)	10, 15, 20
T_{Si}	Poly-Si body thickness (nm)	5, 7.5, 10, 15
T_{OX}	Equivalent oxide thickness (nm)	12.6
N_A	Channel doping concentration (cm^{-3})	10^{17}
N_D	S/D doping concentration (cm^{-3})	5×10^{19}
N_{GB}	Grain boundary trap states ($cm^{-2}\,eV^{-1}$)	10^{12}–10^{14}
N_{IT}	Si/SiO_2 interface trap states ($cm^{-2}\,eV^{-1}$)	$1, 3, 5\times10^{11}$

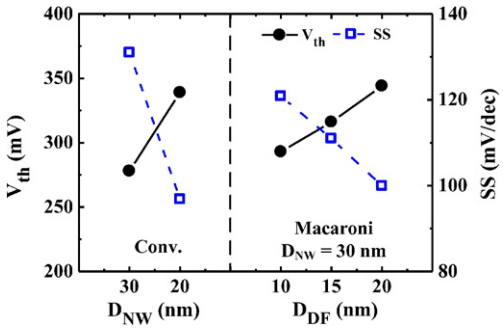

Fig. 2. The V_{th} and SS of the conventional and the macaroni structure with various channel diameters (D_{NW}) and dielectric filler diameters (D_{DF}) without considering the single grain boundary and interface traps in the channel.

Fig. 3 shows the V_{th} and SS variation of the devices due to SGB or RITs in the channel. When considering only the SGB in the channel ($D_{NW} = 30$ nm), the macaroni structure shows less V_{th} and SS variations suggesting the effective suppression of the SGB effect by the DF. As the D_{DF} increases, the number of SGB traps in the channel decreases and thus electrical variation can be reduced. However, although the conventional with $D_{NW} = 20$ nm has smaller SGB traps than that of the macaroni structure ($D_{DF} = 20$ nm), the V_{th} and SS variations of the conventional ($D_{NW} = 20$ nm) are more severe than that of macaroni $D_{DF} = 20$ nm. This result indicates that the grain boundary trap in the macaroni structure can have different roles in the channel.

For further understanding of the effect of the SGB in the channel, the potential profiles between the conventional ($D_{NW} = 20$ nm) and the macaroni ($D_{DF} = 20$ nm) are compared. Fig. 4 shows the conduction energy band (E_C) along the channel both of the conventional and the macaroni structures at a fixed $V_G = 0.4$ V ($\approx V_{th}$) and $V_D = 0.05$ V. Fig. 4(a) shows the cross-sectional E_C of both devices and Fig. 4(b) is the E_C profile along the channel region at 2 nm distance from the gate oxide, as indicated by the black line in Fig. 4(a). The potential barriers due to the SGB are as low as 79.6 meV for the conventional ($D_{NW} =$ 20 nm) and 75.2 meV for the macaroni ($D_{DF} = 20$ nm), respectively. Thus, the macaroni can reduce not only the SGB trap number in the channel but also the potential barrier due to thinner channel thickness.

The number of RITs is proportional to the area of the poly-Si/SiO_2 interface and thus the thicker the conventional devices, the larger the V_{th} and SS variation. For the macaroni structures, they inherently have the additional channel/SiO_2 interface and show larger variation than that of the conventional structures, as shown in Fig. 3. As the D_{DF}

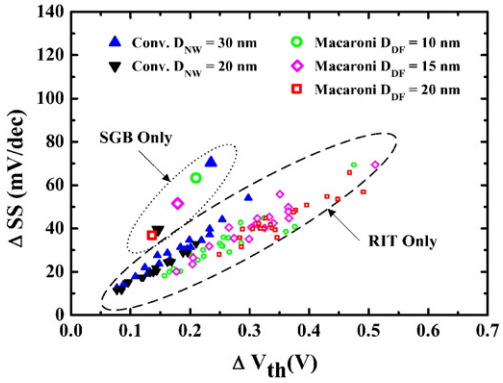

Fig. 3. The V_{th} and SS variation (ΔV_{th} and ΔSS) with various D_{DF} and D_{NW} ($N_{IT} = 5\times10^{11}$ $cm^{-2}\,eV^{-1}$) due to the SGB or the RITs. The $D_{NW} = 30$ nm (blue up triangle) and 20 nm (black down triangle) for the conventional structure (Conv.), and the $D_{DF} =$ 10 nm (open green circle), 15 nm (open magenta diamond) and 20 nm (open red square) for the macaroni structure (Macaroni).