



Graphene/lead-zirconate-titanate ferroelectric memory devices with tenacious retention characteristics



Sejoon Lee ^{a, b, *}, Youngmin Lee ^b

^a Department of Semiconductor Science, Dongguk University - Seoul, Seoul 04623, Republic of Korea

^b Quantum-Functional Semiconductor Research Center, Dongguk University - Seoul, Seoul 04623, Republic of Korea

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ABSTRACT

With the motivation of realizing the high performance graphene-based nonvolatile memory devices, we fabricate and characterize reliable and robust ferroelectric field-effect transistor (FFETs), which are composed of single-layer graphene (SLG) and lead-zirconate-titanate (PZT). After completing all of the fabrication steps, the samples are annealed in vacuum to improve the device characteristics. Through systematic analyses, we investigate an optimal vacuum-annealing condition for improving the memory characteristics of the device. At annealing temperatures at 250–300 °C, both the electrical conduction properties of the SLG channel and the capacitive-coupling abilities of the SLG/PZT/Pt stack are dramatically improved because of the elimination of chemical residues and/or molecular oxygens. Consequently, the vacuum-annealed SLG-PZT FFET displays a great improvement of data retention (~72% after 10 year) and a large memory window (~4.1 V). We believe the present study can provide alternative avenues for exploring unprecedented graphene-based memory structures.

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1. Introduction

Graphene has attracted tremendous attention because of its extraordinary physical properties [1,2]; such as a linear dispersion of the electron energy, a high carrier mobility at room-temperature, a high mechanical strength of the sp² carbon array, and a high transparency of the two-dimensional lattice-structure. Owing to these excellent characteristics, plenty of functional devices have been suggested and demonstrated to move a step closer to future electronics [3–6]. Among various electronic devices, graphene-based non-volatile memories are of great interest [7] because graphene serves several exceptional advantages over the conventional Si-based memory devices (e.g., high feasibility of the transparent-flexible device scheme [8], low cell-to-cell interference [9], large memory window [10–12], high gate capacitive-coupling strength [13] etc.). One of the most prospective candidates for the high-performance graphene-based non-volatile memory is a graphene ferroelectric field-effect-transistor (FFET). When implementing graphene into the FFET structure, graphene can provide a distinctive advantage over conventional semiconductors because

the two-dimensional nature and the absence of dangling bonds offer a non-reactive robust interface with the substrate. In addition, since graphene can be placed directly on the ferroelectric material, an additional sacrificial dielectric layer is unnecessary, different with conventional semiconductor FFETs. Furthermore, the two-dimensionality of graphene renders an absence of depletion capacitance, which can further restrict the strength of capacitive coupling between the ferroelectric oxide and the channel material. These improve the device characteristics of the graphene FFETs (e.g., low operating voltage, large memory window etc.) [13–16]. In graphene-based memory devices [8–16], however, a meager data-retention has been often observed because of depolarization effects and/or voltage drops, arising from interface states [13] and/or molecular impurities [16] at the graphene/ferroelectric-oxide interface. Such an insubstantial retention is closely associated with chemical adsorbates (e.g., H₂O, O₂, NO₂, NH₃, CO, resist residues of etc.) [17–20], which might be introduced during the graphene-transfer and/or the fabrication steps. In recent years, fortunately, it has been reported that those adsorbates could be effectively desorbed through thermal annealing [20–25] or chemical treatments [26]. This give us a hint to improve the device characteristics and to study more insights of the graphene FFET for better understanding and potential use of graphene-based non-volatile memory devices. In light of this, we have investigated the

* Corresponding author. Department of Semiconductor Science, Dongguk University - Seoul, Seoul 04623, Republic of Korea.

E-mail address: sejoon@dongguk.edu (S. Lee).

effects of thermal annealing on the memory characteristics of the graphene FFETs.

In this article, we fabricate the graphene FFETs using single-layer graphene (SLG) and lead-zirconate-titanate (PZT), and characterize their physical properties. The SLG-PZT FFETs are fabricated through conventional photo-lithography techniques, and those are subsequently annealed in vacuum to improve the device characteristics. The effects of thermal annealing on the physical properties of the SLG-PZT FFETs are systematically examined, and the mechanisms of the improved device properties are discussed.

2. Experimental details

2.1. Preparation of SLG/PZT/Pt/SiO₂/Si substrates

Fig. 1(a) schematically illustrates the device structure of the fabricated SLG-PZT FFET. To construct such a structure, first, the 180-nm-thick PZT layer was synthesized on the 200-nm-thick Pt (111)/SiO₂/Si substrate by 6-times-repeated sol-gel processes [27,28]. Then, the sample was annealed at 550 °C for 120 s in O₂ to improve the crystal quality of PZT. Next, the SLG sheet was grown on Cu foil using a chemical vapor deposition (CVD) method [29,30] and transferred onto the surface of the PZT/Pt/SiO₂/Si substrate using a poly (methyl methacrylate) transfer method [31].

2.2. Fabrication and thermal treatments of PZT-SLG FFETs

The PZT-SLG FFETs were fabricated using the SLG/PZT/Pt/SiO₂/Si substrates. The SLG channels (l : 12 μm , w : 2 μm) were patterned via photolithography techniques, and the source/drain areas were defined through forming Ti/Au electrodes by e -beam evaporation and lift-off methods. The Pt layer underneath the PZT was used as the gate electrode. After the fabrication of PZT-SLG FFETs, the samples were annealed at 200–350 °C for 10 min in a resistance-heated oven under high vacuum ambience ($\sim 10^{-6}$ Torr).

2.3. Characterization of SLG, PZT, and PZT-SLG FFETs

The Raman scattering characteristics of the as-prepared and annealed SLG samples were measured by using a Renishaw Micro

Raman microscope system. An acquisition time of 600 s was used with a 514-nm laser. The power density for laser irradiation was less than 2 mW/ μm^2 . To specify the Raman scattering properties of the SLG channel region (w : 2 μm , l : 12 μm), we fixed the size of the scanned area at 2 μm in diameter. The ferroelectric properties of PZT were examined by polarization vs. voltage (P-V) measurements using a home-built Sawyer-Tower system equipped with an Agilent 33120 A function generator. The electrical properties of the PZT-SLG FFETs were measured at room temperature in a vacuum environment (3.0×10^{-6} Torr) by using a Keysight B1500A semiconductor device parameter analyzer.

3. Results and discussion

Fig. 1(b) shows the P-V characteristic curves of the reference sample of PZT (*i.e.*, Pt/PZT/Pt). The sample clearly exhibits the ferroelectric hysteresis loops, and the loops become larger and clearer as the sweep-voltage (V_{sweep}) increases. When $V_{\text{sweep}} = 7$ V, the coercive field and the remnant polarization are ~ 120 kV/cm and ~ 22 $\mu\text{C}/\text{cm}^2$, respectively. The Raman characteristics of the CVD-grown SLG are shown in Fig. 1(c). The Raman spectrum of SLG represents only two distinctive features from G and 2D bands in graphene. The high intensity ratio of I_{2D}/I_G (>2) depicts high-quality of SLG [32]. The absence of delamination, wrinkles, and particles in a large domain size (>30 μm^2) further corroborates high-quality of our SLG (see the inset of Fig. 1(c)). Fig. 1(d) displays the optical microscope image of the SLG-PZT FFETs fabricated using the SLG/PZT/Pt/SiO₂/Si substrate, where the channel areas (l : 12 μm , w : 2 μm) are well defined with no visible distortion and delamination of SLG.

Soon after completing all of the device fabrication steps, we carried out thermal annealing of the samples in vacuum and investigated the effects of the annealing temperature (T_a) on the characteristics of the devices. Fig. 2(a) shows the Raman spectra of the SLG channels for the as-prepared and the annealed SLG-PZT FFETs. All of the samples reveal an identical Raman feature of high-quality SLG (*i.e.*, only two G and 2D single-Lorentzian peaks). First, the absence of the defect-related D band (≈ 1350 cm^{-1}) depicts that vacuum-annealing at given temperatures induces no damage to the sp^2 -hybridized carbon structure of graphene. In addition, most of the samples still maintain a high intensity ratio of I_{2D}/I_G over 2.5, except for the 350 °C-annealed sample (see also Fig. 2(b)). These indicate that, at $T_a = 200$ – 300 °C, the SLG channels patterned on PZT seldom interact with oxygens and/or other species of the substrate.

Here, it is necessary to perceive the variation of the G band's peak position (G_{peak}) upon varying T_a . For the as-prepared SLG channel, G_{peak} appears at 1588.3 cm^{-1} . The observed G_{peak} position is blue-shifted from pristine graphene ($G_{\text{pristine}} \approx 1580$ – 1584 cm^{-1}) [23,33] because of hole-doping from chemical residues [19,20] and/or molecular oxygens [18], which might be adsorbed onto and/or underneath SLG during the transfer and the fabrication steps. However, as plotted in Fig. 2(b), G_{peak} is gradually red-shifted with increasing T_a up to 300 °C. This implies that the unintentional acceptors (*i.e.*, chemical residues and/or molecular oxygens) are effectively removed via thermal annealing at 200–300 °C because the red-shift of G_{peak} toward G_{pristine} corresponds to the decrease in the impurity-induced in-plane vibration of sp^2 carbon atoms. When T_a increases up to 350 °C, however, G_{peak} is suddenly blue-shifted to 1592.4 cm^{-1} . This can be attributed to the monotonic variation of the electronic structure of SLG due to hole-doping in graphene [18,21,22], possibly resulting from the reaction with oxygen atoms in PZT.

The alterations of the Raman scattering characteristics are closely related to the electrical properties in the SLG channels

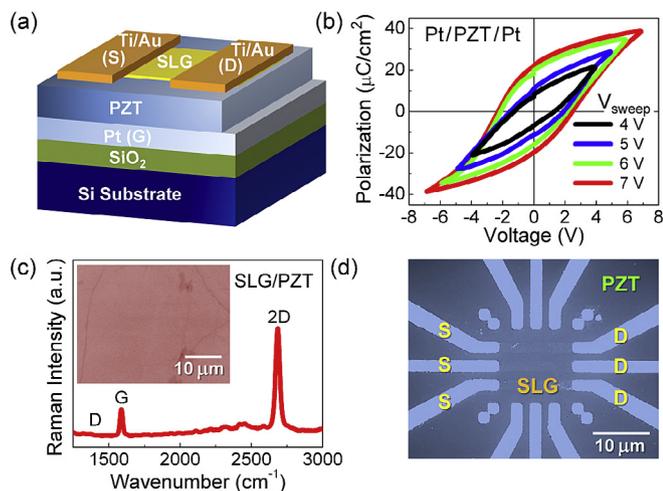


Fig. 1. (a) Schematic configuration of the SLG-PZT FFET memory device structure. (b) P-V characteristic curves of PZT measured from the reference sample of Pt/PZT/Pt. (c) Raman spectrum of SLG. The inset display the scanning electron microscopy image of the SLG surface transferred onto the PZT substrate. (d) Optical microscope image of the SLG-PZT FFET devices. (A colour version of this figure can be viewed online).

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