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Properties of synthetic epitaxial graphene/molybdenum disulfide lateral heterostructures

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ABSTRACT

Graphene has been proposed as a high-quality contact to two-dimensional (2D) transition metal dichalcogenides (TMDs) for the development of "all 2D" devices. Here, we demonstrate the direct-growth of epitaxial graphene (EG) based lateral heterostructures where the EG acts as a directly grown contact to a molybdenum disulfide (MoS_2) channel. Utilizing a "seed-free" process, the nucleation of MoS_2 occurs at the lateral substrate/graphene interface, and subsequently grows outward from the edge of the graphene. Transmission electron microscopy (TEM) of the heterostructure provides the first direct observation that a pristine vertical overlap of MoS_2 on graphene exists, instead of previously reported horizontal stitching, and demonstrates full preservation of the van der Waals gap in the overlap region. Electrolytic gating of the MoS_2/EG heterostructures provides evidence that EG can significantly improve transport compared to the traditional metal/MoS_2 junctions, reducing contact resistance by > 10x, while reducing the sheet resistance by ~ 70%.

1. Introduction

Growth of transition metal dichalcogenides (TMDs) has been studied for decades [1,2], with the most recent interest focused on integrating monolayer forms of these novel materials [3] into electronic devices. A primary challenge to realizing high performance devices based on TMDs is the development of low resistance, ohmic contacts [4]. There have been a wide variety of studies focused on various metals and their combinations to improve contacts to the TMDs [5], but most metals increase interfacial resistances compared to using graphene [6,7]. Das et al. have demonstrated that exfoliated graphene can provide a low resistance contact to WSe_2 as compared to conventional metals [8] because graphene leads to smaller work-function differences, which reduces the barrier to electron transport [9,10]. This was even the case with non-ideal interfaces often found in exfoliated crystalline materials. The initial exfoliation work [11,12] was followed by the direct synthesis of lateral heterostructures based on a combination of different TMDs and chemical vapor deposited (CVD) graphene [13–15]. In these cases, the CVD graphene is initially transferred from a copper or nickel substrate to silicon dioxide/silicon (SiO_2/Si) substrates to allow for back gating of the TMD, and graphene is used as source and drain contacts. Growth of the TMD also often employs a "seed" such as perylene-3,4,9,10-tetracarboxylic acid tetrapotassium salt (PTAS), which promotes nucleation randomly across the sample [13,15,16]. As often noted for polymer-assisted transfer processes [17], the transferring of CVD graphene traditionally leads to polymer contaminants that can ultimately impact the TMD/graphene interface transport properties [13–15].

Here, we present the use of epitaxial graphene (EG) — graphene grown from silicon carbide (SiC) via silicon sublimation — as the building block for 2D lateral heterostructures. The use of EG and a seed-free synthesis of MoS_2 via powder vaporization minimizes a variety of contamination sources by eliminating polymer transfers

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and organic seed layers typically used in lateral heterostructure syntheses. The MoS_2 nucleates and grows along the patterned graphene edge, with a preference to grow in the etched regions as opposed to on the EG. Transmission electron microscopy (TEM) verifies that the MoS_2/EG interface is vertically stacked rather than horizontally stitched, and indicates a pristine van der Waals interface. Finally, we demonstrate a >10x decrease in EG/MoS_2 contact resistance compared to conventional titanium/gold (Ti/Au), along with a reduction in the sheet resistance by ~ 70% upon introduction of the EG as the contact. It is envisioned that these pristine, as-grown graphene contacts are a milestone on the path to making 'all-2D' electronics a scalable reality.

2. Experimental section

The experimental procedure for the fabrication of the EG/MoS_2 heterostructure is graphically represented in Fig. 1. The following subsections describe the process of graphene synthesis, patterning, MoS_2 synthesis, and device fabrication.

2.1. Synthesis of graphene and molybdenum disulfide (MoS_2)

Epitaxial graphene (EG) is grown via silicon sublimation from the silicon face of 6H silicon carbide (SiC (0001)) [18] (Fig. 1a,b) in a three-phase, hot-zone, graphite furnace (Thermal Technology LLC). The SiC is first cleaned using acetone, isopropyl alcohol and Nanostrip™. Subsequently, the SiC is annealed in 10% hydrogen (balance argon) at 1500 °C for 30 min to remove subsurface damage due to chemical and mechanical polishing [18]. The H_2 is then pumped from the system, and the temperature is increased to 1800 °C for 10 min at 500 Torr to form the graphene layers. This process yields low defect density multi-layer EG (See supplementary section S.1).

Following graphene growth and patterning (Fig. 1c,d and section 2.2), MoS_2 is synthesized using powder vaporization (Fig. 1e). This is also referred to as chemical vapor deposition (CVD) in other literature [16,19], but given the lack of preciseness of this process compared to traditional CVD [20], we choose to refer to it as "powder vaporization". In this case, patterned graphene substrates are placed on top of a rectangular crucible containing 2–3 mg of molybdenum trioxide (MoO_3) powder and into the hot zone of a quartz tube furnace. Subsequently, 300 mg of sulfur (S) powder was placed approximately 27 cm upstream from the hot zone. The system is purged with argon prior to growth, and sulfur is independently heated to 130 °C once the hot zone reaches 500 °C to provide a continuous sulfur flow during the MoS_2 growth, which occurs at 800 °C for 20 min [21].

2.2. Graphene patterning

Graphene ribbons are patterned on the substrate using standard ultraviolet (UV) photolithography as shown in Fig. 1c and d. A pattern consisting of varied channel spacing constituting a transfer length method (TLM) pattern [22] is produced using a photoresist double stack (PMGI SF2 + SPR 3012) exposed using a Stepper 8500. A subsequent mixture of oxygen and argon (O_2/Ar) is used for a reactive ion etch to remove the EG outside of the patterns [23], leaving behind a series of periodically spaced graphene rectangles of fixed width, that ultimately constitute the contacts to the MoS_2 channel for transistor fabrication. In addition to removing EG, this etch recipe also oxidizes the SiC substrate (see discussion and supplementary section S.4) based on TEM and x-ray photoelectron spectroscopy (XPS). The lithographic mask is designed so that EG is completely removed in specific regions on the SiC substrate to provide areas where MoS_2-only (without the graphene contacts) is grown for benchmarking purposes.

2.3. Heterostructure device fabrication

To prevent unwanted current flow, the heterostructures are lithographically patterned into isolated channels (Fig. 1f, g and 1h). A sulfur hexafluoride (SF_6)/O_2 reactive ion etch [24] effectively removes the excess MoS_2, thereby isolating any MoS_2 growth strictly between the graphene electrodes. Subsequently, contact regions are lithographically patterned, briefly exposed to an O_2 plasma [25], and titanium/gold (5/15 nm) metal is deposited via electron-beam evaporation (Fig. 1i), followed by lift off in PRS 3000 photoresist remover (Fig. 1j and k). Two electrical test structures are produced: 1) the EG/MoS_2/EG lateral heterostructure with the Ti/Au metal contacting the EG (Fig. 1j), and 2) a traditional MoS_2–based structure that is directly contacted by the Ti/Au (Fig. 1k) for benchmarking the performance of the EG as a contact.

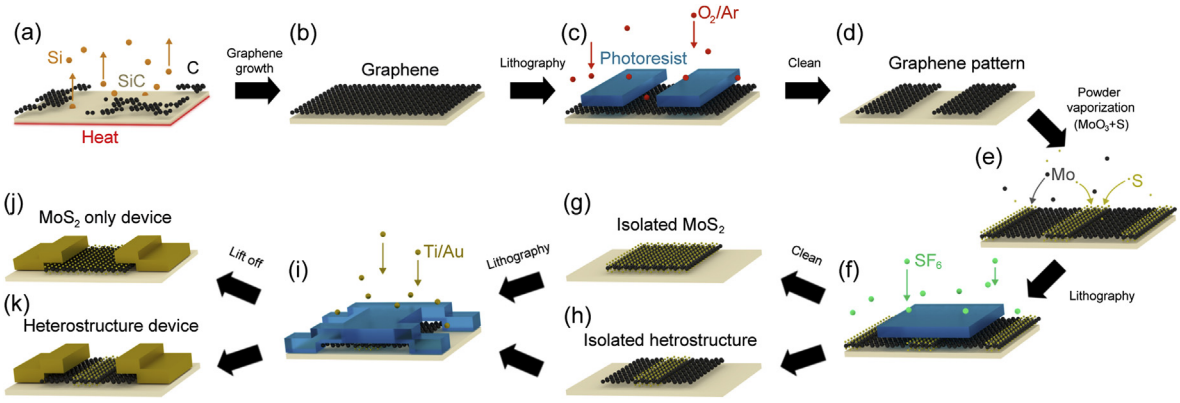

Fig. 1. Process flow of the EG/MoS_2 heterostructure fabrication process – (a) Upon application of heat, the silicon from SiC sublimes and the carbon that is left behind reconstructs to form a uniform layer of graphene as shown in (b). Photolithographic patterning employing a double stack of photoresist (PMGI SF6 + SPR 3012) is used, followed by an O_2/Ar reactive ion etch as in (c). (d) shows the patterned graphene substrate, which is then used to grow MoS_2 via powder vaporization (MoO_3 + S) in a quartz tube furnace. (f) shows photolithographic patterning and exposure to an SF_6 plasma to create isolated heterostructure channels, as in (h) and prevent unwanted current flow. (g) shows a similar control isolated channel of only MoS_2. Step (i) shows the photolithographic patterning and electron-beam deposition of Ti/Au (5/15 nm) which is subsequently followed by lift-off in cleaning solvents (acetone followed by PRS 3000) to obtain the two test devices: (j) MoS_2-only device; and (k) EG/MoS_2/EG back-to-back heterostructure device. (A colour version of this figure can be viewed online.)