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High performance full subtractor using floating-gate MOSFET

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ABSTRACT

Low power consumption has become one of the primary requirements in the design of digital VLSI circuits in recent years. With scaling down of device dimensions, the supply voltage also needs to be scaled down for reliable operation. The speed of conventional digital integrated circuits is degrading on reducing the supply voltage for a given technology. Moreover, the threshold voltage of MOSFET does not scale down proportionally with its dimensions, thus putting a limitation on its suitability for low voltage operation. Therefore, there is a need to explore new methodology for the design of digital circuits well suited for low voltage operation and low power consumption. Floating-gate MOS (FGMOS) technology is one of the design techniques with its attractive features of reduced circuit complexity and threshold voltage programmability. It can be operated below the conventional threshold voltage of MOSFET leading to wider output signal swing at low supply voltage and dissipates less power as compared to CMOS circuits without much compromise on the device performance. This paper presents the design of full subtractor using FGMOS technique whose performance has been compared with full subtractor circuits employing CMOS, transmission gates (TG), complementary pass transistor logic (CPL) and gate diffusion input (GDI). It has been observed that the FGMOS based full subtractor uses minimum number of transistors (10) while consuming least power (1.61×10^{-9} W) with lowest propagation delay (10.62 ps) and power delay product (0.17×10^{-19} Js) besides occupying minimum surface area (0.25×10^{-7} cm^2) in comparison to CMOS, TG, CPL and GDI based full subtractors available in literature, thus suitable for swift miniaturized applications.

1. Introduction

The current trend in consumer electronics strives to achieve low voltage and low power circuit design having utility in portable electronics. The design of digital VLSI circuits has been continuously evolving and being motivated by design criteria such as low power consumption, high speed and small chip area [1–3]. Floating-Gate MOSFET (FGMOS) has been proposed for the design of low voltage and low power applications both in analog and digital circuits owing to its multiple input gates and a unique feature of threshold voltage tunability [4,5]. As a consequence, the characteristics of FGMOS based circuits can be altered by varying the threshold voltage using a bias voltage and hence provides tunability to the circuit. Further, due to multiple input gates which are capacitively coupled to the device, we can apply a number of input signals and their addition in voltage form can be performed [6–8]. In this paper, the design of full subtractor using FGMOS has been presented and its performance has been compared with circuits reported in the literature in terms of parameters such as power, delay, power delay product and transistor count [10]. Although, gate diffusion input (GDI) circuits can be implemented with less transistors to reduce power but it suffers from reduced voltage swing at the output as reported in [11]. FGMOS allows the design of full subtractor with fewer transistors and shows significant improvement in performance parameters such as power, area and speed with wider output voltage swing. The workability of proposed full subtractor has been ascertained by PSpice simulations using level 7 parameters in 0.13 μm CMOS technology with supply voltage of 1 V.

2. Design of full subtractor using FGMOS

The full subtractor is a combinational circuit which performs subtraction using three bits named as A (minuend), B (subtrahend) and B_{in} (borrow bit) from the previous stage yielding outputs as Difference and Borrow. The circuit of full subtractor using FGMOS is shown in Fig. 1 where M1 and M2, M3 and M4, M7 and M8 are multi-input floating-gate MOSFETs, M5 and M6, M9 and M10 are standard CMOS inverters required to complement the outputs from V_2 and V_3 respectively.

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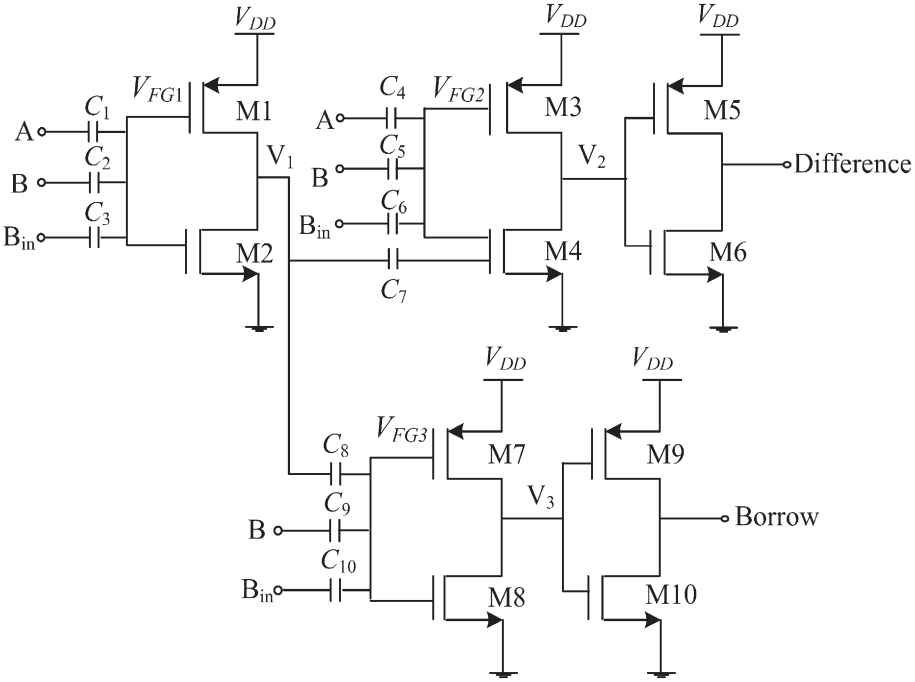

Fig. 1. Full subtractor using FGMOS inverter.

The voltage on the floating gate of first inverter M1-M2 is given by [9]:

$$V_{FG1} = \frac{AC_1 + BC_2 + B_{in}C_3}{C_1 + C_2 + C_3} \tag{1}$$

where C_1, C_2 and C_3 have been assumed 0.1 pF giving

$$V_{FG1} = \frac{A + B + B_{in}}{3} \tag{2}$$

The output of first inverter (V_1) becomes low when V_{FG1} goes above the threshold value (V_{th}) of M2. The threshold voltage $V_{th} = 0.43$ V has been obtained from the transfer characteristics of *n*-channel FGMOS at a reference current of 0.1 μA.

Now, the voltage on the floating gate of second inverter M3-M4 is given by:

$$V_{FG2} = \frac{AC_4 + BC_5 + B_{in}C_6 + V_1C_7}{C_4 + C_5 + C_6 + C_7} \tag{3}$$

$$V_{FG2} = \frac{A + B + B_{in} + 2V_1}{5} \tag{4}$$

(For $C_4 = C_5 = C_6 = 0.1$ pF and $C_7 = 0.2$ pF).

Also, the voltage on the floating gate of third inverter M7-M8 is given by:

$$V_{FG3} = \frac{V_1C_8 + BC_9 + B_{in}C_{10}}{C_8 + C_9 + C_{10}} \tag{5}$$

where $C_8 = C_9 = C_{10} = 0.1$ pF and we have

$$V_{FG3} = \frac{V_1 + B + B_{in}}{3} \tag{6}$$

Table 1 give the truth table of the proposed full subtractor besides the values of V_{FG1}, V_{FG2} and V_{FG3} compared to threshold voltage for each input combination.

Now, the circuit of full subtractor using FGMOS has been simulated by selecting *W*/*L* of p-channel MOSFETs as 2.6 μm/0.13 μm and n-channel MOSFETs as 1.3 μm/0.13 μm with supply voltage of 1 V. The timing diagrams of proposed full subtractor for various input combinations are shown in Fig. 2.

As evident from the Fig. 2, the proposed circuit of full subtractor shows rail to rail output signal swing due to reduced threshold barrier at low supply levels leading to improved noise immunity and may also eliminate false triggering. Further, the performance of proposed full subtractor has been compared with previous full subtractor designs reported in reference [10]. A comparative performance of proposed full subtractor employing FGMOS with respect to full subtractor employing

Table 1
Truth table of full subtractor.

Inputs			$V_{th} = 0.43$ V							
A	*B*	B_{in}	V_{FG1}	V_1	V_{FG2}	V_2	Difference	V_{FG3}	V_3	Borrow
0	0	0	0 < 0.43	1	0.4 < 0.43	1	0	0.33 < 0.43	1	0
0	0	1	0.33 < 0.43	1	0.6 > 0.43	0	1	0.66 > 0.43	0	1
0	1	0	0.33 < 0.43	1	0.6 > 0.43	0	1	0.66 > 0.43	0	1
0	1	1	0.66 > 0.43	0	0.4 < 0.43	1	0	0.66 > 0.43	0	1
1	0	0	0.33 < 0.43	1	0.6 > 0.43	0	1	0.33 < 0.43	1	0
1	0	1	0.66 > 0.43	0	0.4 < 0.43	1	0	0.33 < 0.43	1	0
1	1	0	0.66 > 0.43	0	0.4 < 0.43	1	0	0.33 < 0.43	1	0
1	1	1	1 > 0.43	0	0.6 > 0.43	0	1	0.66 > 0.43	0	1