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Understanding the dependence of the ohmic drain-source leakage current on gold deposition rate in top-contact pentacene-based thin film transistors

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ABSTRACT

We studied the influence of the gold deposition rate on the drain-source leakage current of top-contact pentacene-based thin film transistors (TFTs) with different channel lengths. It is demonstrated that the anomalous leakage current which occurs only in short-channel TFTs monotonically increases with increasing the gold deposition rate. For TFTs with channel length of 30 μm, we also investigated the dependence of the drain-source leakage current on the pentacene grain size as well as the gold deposition rate. It is shown that the pentacene grain size influences the leakage current only in the case if high gold deposition rate is employed, whereas the anomalous leakage current can be avoided by reducing the gold deposition rate. Finally, due to the observed ohmic character of the anomalous leakage current, we propose that the origin of the current can be attributed to parasitic leakage paths on the surface of the pentacene layers formed by the lateral diffusion of gold clusters from drain/source edges into the channel region during gold deposition. Based on this hypothesis, the observed dependence of the anomalous leakage current on the gold deposition rate can be well explained.

1. Introduction

Advanced organic semiconductor technology is very attractive because it allows the fabrication of innovative devices such as flexible paperlike displays or identification tags at much lower costs compared to conventional silicon technologies [1]. In order to obtain high current output capability and switching speed of electronic circuits, short-channel OTFTs must be fabricated [2]. However, as the channel length decreases, the suppression of the off-current between drain and source electrodes becomes more challenging. An undesirable increase of the so-called anomalous drain-source leakage current has often been reported for short-channel OTFTs [2–10]. Although the origin of the anomalous drain-source leakage current for top-contact pentacene TFTs was discussed in previous works [2,6,7], the underlying physical mechanism is still an open issue.

In this letter, the influence of the gold deposition rate (D_{Au}) on the drain-source leakage current ($I_{L,DS}$) of top-contact pentacene thin film transistors (TFTs) with different channel lengths (L) was investigated, and the corresponding measurement results were analyzed. In addition, the dependence of $I_{L,DS}$ on the pentacene grain size (A_{Pen}) induced by the different pentacene deposition rates (D_{Pen}) for TFTs with channel length of 30 μm was examined. Finally, to explain the observed linear relationship between the anomalous leakage current and the drain voltage (V_{DS}), we propose a hypothesis that the lateral diffusion of gold clusters on the surface of pentacene layers from drain/source edges into the channel region possibly forms parasitic leakage paths between drain/source electrodes during gold deposition, increasing the off-current.

2. Device Fabrication

Top-contact pentacene TFTs as shown in Fig. 1(a) were fabricated on an arsenic-doped silicon wafer (resistivity = 0.001–0.005 Ω cm) with a 300-nm-thick silicon dioxide (SiO_2), which forms the gate and the dielectric layer, respectively. Prior to the pentacene film deposition, substrates cut from the same wafer with SiO_2 dielectric layer were rinsed with acetone and isopropanol sequentially in an ultrasonic bath for 10 min each, and then were wet cleaned with deionized water, blown with a nitrogen gun and heated at 120 °C for 1 h in a dry nitrogen atmosphere.

Based on these substrates we fabricated two sets of transistors in a glove box (*MBraun*) with O_2 and $H_2O < 0.1$ ppm. The first set (Set I) was used to investigate the influence of D_{Au} on $I_{L,DS}$ for different values of L. For the preparation of Set I, a 30-nm-thick layer of pentacene (sublimed grade and purity = 99.9%) purchased from Sigma-Aldrich was thermally evaporated onto the substrates at a rate of D_{Pen} = const. = 0.30 Å/s in a vacuum chamber at about 10^{-6} mbar to form

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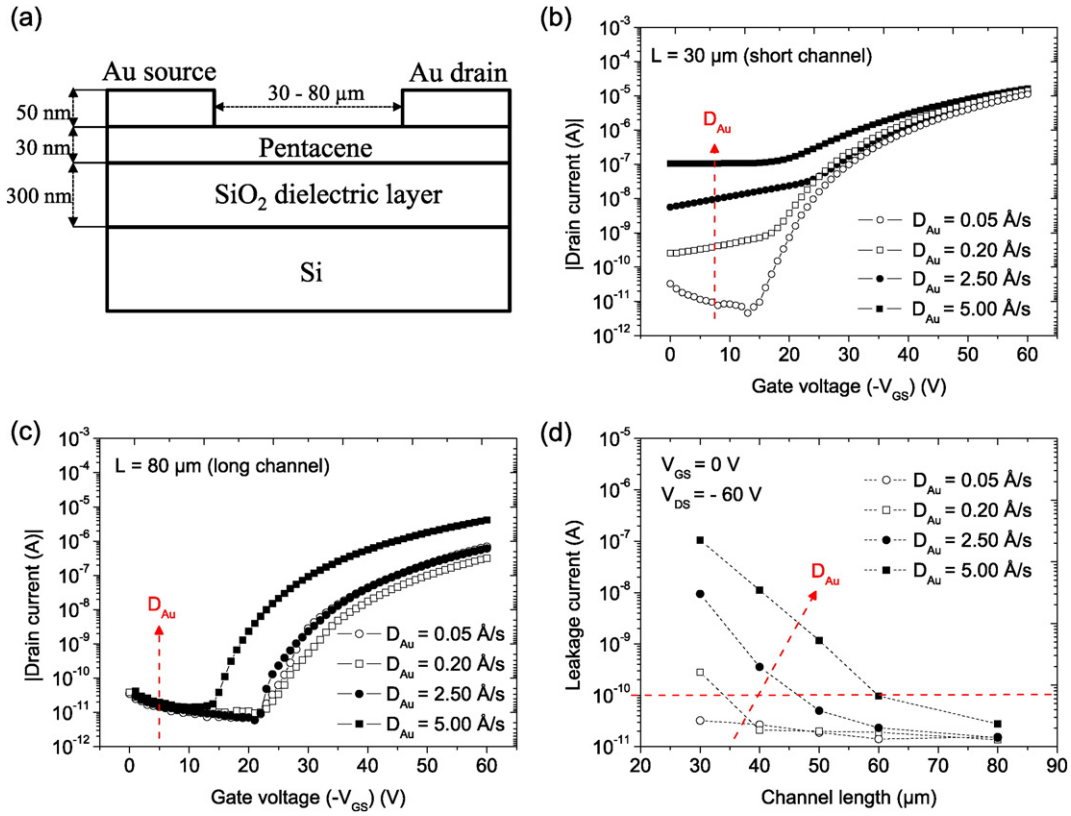

Fig. 1. (a) Schematic of transistor cross-section. Transfer characteristics ($V_{DS} = -60$ V) for top-contact pentacene TFTs fabricated with different D_{Au} ranging from 0.05 to 5.00 Å/s based on various L (b) L = 30 µm, (c) L = 80 µm. (d) Leakage current ($V_{DS} = -60$ V, $V_{GS} = 0$ V) plotted as a function of L and D_{Au}.

the active layer. A 50-nm-thick gold (Au) contact layer was then deposited onto the active layer by thermal evaporation through a hard-electroformed-nickel-based shadow mask (35 µm as thickness) to define five transistors with the same channel width (W = 1 mm) and different channel lengths (L) in the range from 30 to 80 µm. The deposition rate for the creation of the gold contacts was varied in the range from 0.05 to 5.00 Å/s. The substrate temperature during the gold deposition was maintained at room temperature (25 °C) using a water-cooling system.

A second set (Set II) of transistors was prepared to further investigate the dependence of $I_{L,DS}$ on A_{Pen} for TFTs with channel length of 30 µm. For the fabrication of Set II pentacene layers with a thickness of 30-nm were thermally evaporated onto the substrates at two different rates ($D_{Pen} = 0.12$ Å/s, $D_{Pen} = 1.20$ Å/s) resulting in different pentacene grain sizes A_{Pen}. Then, 50-nm-thick gold contact layers were deposited on the pentacene layers at two various rates ($D_{Au} = 0.05$ Å/s, $D_{Au} = 5.00$ Å/s) for each different grain size.

All electrical measurements of the pentacene TFTs were performed using an Agilent 4156C semiconductor parameter analyzer in the glove box. After completion of the electrical measurements, atomic force microscopy (AFM) in non-contact mode was used to measure the surface morphology of the pentacene layers in air.

3. Results and discussion

The transfer characteristics for both, short-channel (30 µm) and long-channel (80 µm) TFTs with different D_{Au} from Set I are shown in Fig. 1(b) and (c), respectively. We observed an increase of the drain-source current $I_{L,DS}$ in the off-state with increasing D_{Au} for the short-channel transistors (L = 30 µm), whereas $I_{L,DS}$ is negligible ($<10^{-10}$ A) for the long-channel transistors (L = 80 µm). To further investigate this behavior the leakage currents $I_{L,DS}$ measured at $V_{DS} = -60$ V and $V_{GS} = 0$ V for TFTs with different channel lengths L are plotted in Fig. 1(d) for different values of D_{Au}. The figure shows that the anomalous leakage current can only be observed when L is short (L < 60 µm). In these cases $I_{L,DS}$ monotonically increases with increasing D_{Au}. This implies that for long-channel transistors the anomalous leakage current is negligible, and for short-channel transistors the anomalous leakage current can be eliminated by decreasing the gold deposition rate D_{Au}, thus indicating that the gold deposition rate is a crucial factor which strongly influences the anomalous leakage current.

The above-mentioned increase of the anomalous leakage current with decreasing L was also observed in a previous work [2], however it was found that this behavior only reproducibly occurred for large-grain pentacene TFTs, but not for small-grain TFTs, indicating that the anomalous leakage current is also dependent on the pentacene grain size A_{Pen}.

To investigate whether A_{Pen} or D_{Au} is the dominant factor for the anomalous leakage current, we measured the short-channel (30 µm) TFTs from Set II where the pentacene deposition rate D_{Pen} was used to adjust the pentacene grain size A_{Pen}. The respective transfer characteristics are shown in Fig. 2. The insets in Fig. 2 exhibit the different surface morphology of the pentacene layers deposited by various D_{Pen} and show that A_{Pen} can be adjusted by varying D_{Pen}. It can be seen that the pentacene grain size has an influence on the leakage current only in the case of high gold deposition rate. The transistors fabricated with a low gold deposition rate exhibit the negligible anomalous leakage current, which is consistent with the result we have obtained above (see Fig. 1d) and which leads to the conclusion that the gold deposition rate is the dominant factor for determining the anomalous leakage current.

In terms of possible explanations for describing the physical origin of the anomalous leakage current, previous works considered a space-charge-limited current (SCLC) as well as a current caused by field