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Thermal assessment of copper through silicon via in 3D IC

Younhwan Shin [a], Sarah Eunkyung Kim [b], Sungdong Kim [a,*]

[a] Dept. of Mechanical System Design Eng., Seoul National University of Science and Technology, Seoul, Republic of Korea
[b] Graduate School of NID Fusion Technology, Seoul National University of Science and Technology, Seoul, Republic of Korea

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ABSTRACT

Thermal management in 3D IC is an important factor in terms of IC performance and reliability. In this study, the feasibility of Cu TSV as a heat dissipation path was experimentally investigated. Si wafers with or without Cu TSV were point-heated at various temperatures and thermal diffusion in the specimens was observed using IR microscope. Si wafers with Cu TSV showed higher top surface temperature than ones without Cu TSV as the heating power increased. This phenomenon was attributed to the preferred heat transfer through Cu TSV in the vertical direction due to high thermal conductivity of Cu. This implies that Cu TSV is an effective vertical heat dissipation path.

1. Introduction

Semiconductor industry has increased integrate circuit (IC) density by downscaling IC, which has required state of the art technologies. However, instead of shrinking IC, three-dimensional IC (3D IC) technology stacks chips in a vertical way to achieve higher density of integration and better performance [1–2]. These vertically stacked chips are usually interconnected via through silicon via (TSV) that enables faster performance by shortening interconnection length. While 3D IC has many advantages over conventional 2D IC, there have arisen new manufacturing and reliability issues, for example, temporary bonding and debonding [3], keep-away-zone around TSV [4], thermal management [5], etc. Thermal management in 3D IC becomes important since power generated in a package increases and the heat from neighboring chips affects IC performance [6]. There have been experimental and numerical efforts to understand how design parameters in chip stacking and TSV affect thermal management [7–11]. For example, Lau [6] investigated the equivalent thermal conductivity of interposer with various TSV parameters based on computational fluid dynamics analysis. Oprins [5] performed thermal experimental and modeling characterization of a packaged DRAM on logic stack. It should be noted that so far most of the researches have been focusing on numerical analysis of thermal performance of 3D IC, which is partly due to experimental difficulties in preparing 3D IC specimens and measurement of temperature profile inside 3D stacks. However, since numerical analysis should be validated by experimental results, insufficient thermal experiment on 3D IC deters the advancement of thermal management of 3D IC. In this study, we experimentally investigated the heat transfer performance of Cu TSV using Infrared (IR) microscopy and discussed the feasibility of TSV as an efficient heat dissipation path.

2. Experiments

Fig. 1 shows the schematic diagram of experimental apparatus. It was designed to point-heat a bottom side of specimen using Cu probe so as to simulate the point-heat source in the IC. Cu cooling plate and fan were attached to the bottom of Teflon holder to minimize collateral radiative and convective heating from Cu probe. Specimens used in this study were categorized into (1) single silicon wafer with or without TSV, and (2) two tier stacked silicon wafers with or without TSV as illustrated in Fig. 2. In both categories, the diameter, pitch and depth of TSV were 8 μm, 200 μm and 40 μm, respectively. TSV was fabricated by conventional methods, i.e., deep reactive ion etching, deposition of SiO_2 liner/Ti buffer/Cu seed layer, and electrochemical deposition of Cu. Total number of TSV were 2116 and they were evenly distributed over the whole specimen, resulting in areal TSV density of 0.1%. The thickness of single silicon wafers was set to 40 μm by backside grinding (Disco, DGP8760) for category 1 and the same was thermo-compressive bonded onto 100 μm Si substrate wafer using Cu bumps for category 2. The Cu bumps were fabricated on top of TSV by sputtering method and lift off process. The height, diameter and pitch of Cu bumps were 1 μm, 50 μm and 200 μm, respectively. All specimen size was 1×1 cm^2. The bottom of all specimens was coated with Au thin film to reflect

* Corresponding author.
E-mail address: sdkim@seoultech.ac.kr (S. Kim).

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unwanted IR from hot Cu probe and top side was spray-coated with carbon to provide black body radiation. This carbon layer was supposed to show only the surface temperature by absorbing parasitic IR from surroundings and directly contacting Cu TSV and Si surface.

Heat, generated by a ceramic plate-heater, was delivered to the bottom of specimen via point-contact with Cu probe and diffused throughout the bulk of specimen. Power applied for the ceramic heater was varied from 1.1 W to 8.1 W and the corresponding temperatures of ceramic heater and Cu probe were summarized in Table 1. The resultant temperature profile at the top surface was observed using IR microscope (FLIR, SC5000), where photons from the specimen were counted and converted into temperature using black body reference (Altair software ver5.91.010). The thermal effects of TSV were analyzed by comparing temperature profiles between specimen with TSV and one without TSV. To ensure the reproducibility of point-contact between Cu probe and the specimen and subsequent measurements, all experiments were repeated at least three times independently and evaluated.

3. Results and discussion

As shown in Table 1, the temperature of tip of Cu probe was lower than that of ceramic heater, which implies not all input power was delivered to the specimen. Since it was hard to measure the exact power delivered to the specimen and the temperature of Cu probe in Table 1 might be slightly changed when Cu probe contacted the specimen, input power was used to indicate the degree of heating throughout this study.

In order to investigate an effect of TSV on thermal diffusion in a Si chip, two kinds of 40 μm thick Si wafers were prepared; one with TSV (TSV wafer) and the other without TSV (bare wafer). Both specimens were point-heated at the bottom side and the top surface temperatures were compared (see Fig. 3). The maximum surface temperatures were found to be same for both specimens at low input powers (1.1 W and 3.2 W). However, TSV wafer began to show higher top surface temperature than bare wafer at 5.5 W and 8.1 W and the temperature difference increased as input power was elevated as shown in Fig. 4(b). At input power of 8.1 W, the difference between maximum temperatures at the center was around 4 °C as illustrated in Fig. 4(a) where top surface temperature was profiled

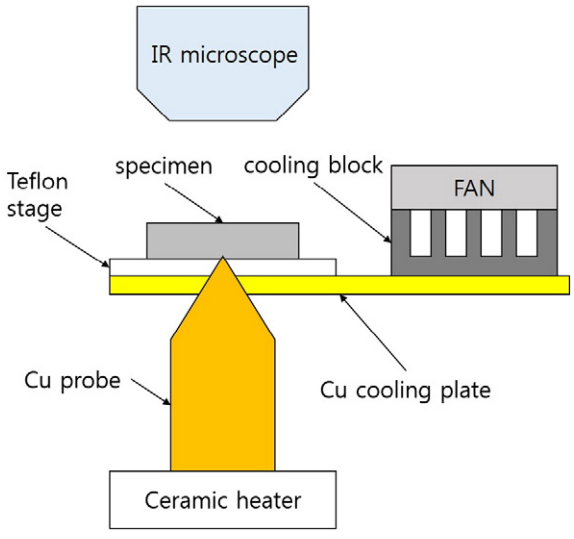

Fig. 1. The schematic diagram of point heating apparatus.

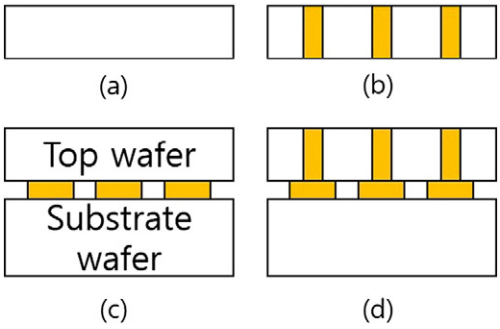

Fig. 2. Illustrative cross sectional view of specimens; (1) single silicon wafer (a) without TSV and (b) with TSV, (2) two tier stacked wafers (c) without TSV and (d) with TSV.

along the line AA′ in Fig. 3(g) and (h). This temperature difference can be ascribed mainly to the thermal effects of TSV but the possibility of overestimation of bare wafer thickness cannot be ignored. Bare wafers having thickness from 40 μm to 720 μm were prepared and the inset of Fig. 4(b) shows how the maximum top surface temperature of bare wafer varies according to the wafer thickness at 8.1 W of input power. Experimental data were fitted with an exponential decay curve and extrapolation of fitting curve showed temperature increment of less than 1 °C at 20 μm thickness. This small increment proves that the possible over or under estimation of bare wafer thickness has negligible effects on the maximum top surface temperature difference.

The maximum top surface temperature depends on the effectiveness of heat transfer from point-heat source to the top surface, i.e. vertical direction heat dissipation. In bare Si wafer, there was only one thermal diffusion path of Si bulk. However, as for the TSV wafer, there were two thermal diffusion paths, i.e., Si bulk and Cu TSV, and Cu is known to have higher thermal conductivity, 385 W/m·K than Si, 149 W/m·K. This additional thermal diffusion path seemed to be more effective as heating power was increased.

Fig. 5 shows top surface temperature of two tiers stacked structure as a function of input power. When 40 μm thick Si wafers (top wafers) were stacked on top of 100 μm thick Si wafers (substrate wafers) using Cu bumps, no significant difference in top surface temperature was observed between top wafer with TSV and one without TSV over all input power range. It was simply because top wafer was heated indirectly through substrate wafer. Due to 100 μm thickness of substrate wafer, top side temperature of substrate wafer was only 74 °C even though it was point-heated at the bottom at around 144 °C. This temperature is too low for Cu TSV to be effective in thermal diffusion as discussed in Fig. 4.

4. Conclusions

Thermal effects of Cu TSV in 3D IC were evaluated using point-heating system and IR microscope. 40 μm thick Si wafer having

Table 1
Input power and corresponding temperatures of ceramic heater and Cu probe.

Input power	Ceramic heater	Tip of Cu probe
1.1 W	50 °C	40 °C
3.2 W	100 °C	72 °C
5.5 W	150 °C	107 °C
8.1 W	200 °C	144 °C