Microelectronic Engineering 156 (2016) 24–29

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Assembly technology development and failure analysis for three-dimensional integrated circuit integration with ultra-thin chip stacking

Chang-Chun Lee [a], Yu-Min Lin [b], Chia-Ping Hsieh [c], Yan-Yu Liou [a], Chau-Jie Zhan [b], Tao-Chih Chang [b], Chien-Ping Wang [a,*]

[a] Department of Mechanical Engineering, Chung Yuan Christian University, 200 Chung Pei Road, Chung Li District, Taoyuan City, 32023, Taiwan, ROC
[b] 3D Stacking and Reliability Technology Department, Electronics and Optoelectronics Research Laboratories, Industrial Technology Research Institute, 195 Sec. 4, Chung-Hsing Road, Chutung, Hsinchu 31040, Taiwan, ROC
[c] Department of Mechanical Engineering, National Taiwan University, No. 1, Sec. 4, Roosevelt Road, Taipei 10617, Taiwan, ROC

ARTICLE INFO

Article history:
Received 27 June 2015
Received in revised form 27 January 2016
Accepted 28 January 2016
Available online 1 February 2016

Keywords:
3D-ICs
Ultra-thin chip
Microbump
FEA
Packaging

ABSTRACT

This study presents a process for wafer handling and robust assembly, which is a novel pre-molding technology applied to assembled stacked modules prior to chip thinning. These steps aim to overcome severe challenges of achieving extra-thin thickness as low as 10 μm for chip stacking in 3D-IC module, such as mechanical damage that appears during chip grinding. A packaging vehicle is fabricated to demonstrate the feasibility of the proposed approach. Analysis results show that underfill flexibility can relieve expansion of the produced stress to establish a 3D simulation model. The top layer of the outermost microjoint has the most serious reliability concern under a load of temperature change. Moreover, failure estimation and mechanical reliability are also performed via 3D nonlinear finite element analysis.

© 2016 Elsevier B.V. All rights reserved.

1. Introduction

Package on package (PoP) and 3D-IC combined with through-silicon vias (TSVs) and microjoints provide excellent solution to the interconnect integration of different chips and assist in achieving high performance [1–3]. Adopting thinned chips is consequently needed to meet the requirements of shrinking the whole thickness of the 3D-IC package. Among the issues in achieving 3D-IC, ultra-thin chip is regarded as an important enabler to provide high-flexibility in dense 3D-IC integrations. Conventional wafer back-thinning techniques are considered high-risk in inducing mechanical damage and fractures during fabrication handling and dicing steps, as well as in the subsequent assembly of chip stacking. Given chip damage in different thinning processes, ball breaker test and three-point bending can be used to measure wafer breaking strength [4–5]. The solution of using narrow cavities underneath chip areas generated via microelectromechanical systems has been provided to overcome this issue [6–7]. However, this approach is difficult for batch manufacture in production and is retardant to the compatibility of current fabricated equipment. Accordingly, the use of temporary handling wafer, adhesive, and laser release integrated into the CMOS harmonious thin wafer process has been developed. Optical four-point bending and electrical test are adopted for verification [8–10]. Moreover, a novel approach of lowering the profile of an ultra-thin package with embedded chip assembled on a Si interposer by lasting chip adhesive bonding style has been presented to maintain chip mounting planarization during assembly [11–12]. Notably, high-density metal lines and electrodes are important to fabricate dual sides of a thin Si interposer without fragile fracture [13], especially for critical interconnected joints, via flip-chip technology. Thermal cycling and four-point bending tests are adopted in the finite element method to evaluate the likelihood of rupture during packaging [14–15]. An example for the bonding strengths and thermal/electrical properties of Cu-Sn microjoints within a stacked module has been described in detail by Lv et al. [16]. Furthermore, adopting wafer level underfill combined with thermal compression method is apparently beneficial to enhance the interconnect reliability of microjoints. The thermal expansion coefficient structure for mechanical failure emerges to prevent pressure during heating [17–18].

The top view for the experimental vehicle of 3D-IC packages with ultra-thin chips are separately shown in Fig. 1. Areas of 5.22 mm × 5.22 mm and 15 mm × 15 mm are applied to assembled stacked chips and a silicon substrate, respectively. The detailed process flows of the pre-molding technology are shown in Fig. 2. For chip stacking (Fig. 1), chips with TSVs, which have blind openings, are first bonded to a wafer level silicon substrate by a reflowed step. Underfill then fills the narrow gap between the chips and the substrate. The next procedure is also pre-filling the molding material. Thinning the sequential stacked

* Corresponding author.
E-mail address: cpwang@cycu.edu.tw (C.-P. Wang).

http://dx.doi.org/10.1016/j.mee.2016.01.040
0167-9317/© 2016 Elsevier B.V. All rights reserved.

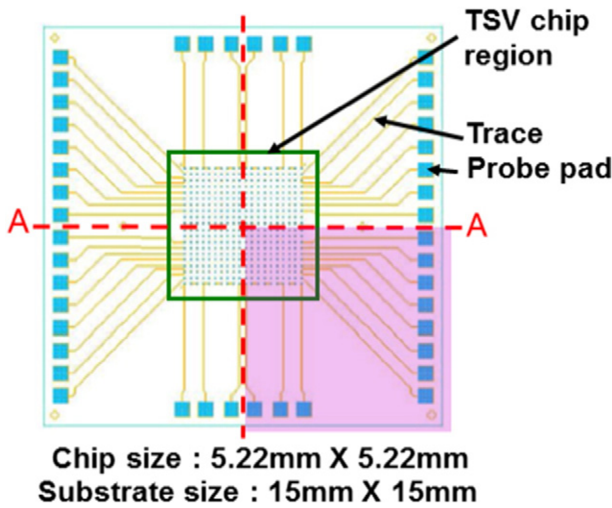

Fig. 1. Top view of the experimental vehicle of 3D-IC packages with ultra-thin chips.

chip by grinding with a mechanical load and reducing the possibility of chip fracture are simplified given structural support from the molding material. Afterwards, the following steps are performed via passivation/opening, bumping, and photo resist strip/etching; an ultra-thin chip assembly is achieved. The fabricated flow is repeated through steps 1 to 9, and a multi-stacked chip can be bonded to construct the considered 3D-IC package.

However, considering that Si chip thickness is ground to several micrometers, rigorous challenges for heterogeneous system integrations and for related thermo-mechanical reliability arise. Such challenges include holding the stacked chips and protecting them from fractured damage before dicing, and implementing sequential assembly processes of 3D-IC packages. To address these issues, this study proposes the assembly approach via pre-molding technology, which is especially suitable for chip to wafer (C2W) bonding technology. The main characteristic of the present assembly approach is the thinning of stacked chips, which is performed after C2W fabrication integrated with pre-filling of molding materials [19–20]. Meanwhile, both chip stacking and concerned packaging structure are completed.

2. Assembled vehicle of 3D-ICs integration

To extract the 3D-IC package, the cross-sectional sketch of chip tacking and the detailed dimensional specifications of the components from the A–A line are presented in Fig. 1. The detailed specifications of the stacked chips with the interconnect system composed of TSVs and microbumps are shown in Fig. 3. Notably, a 230-μm pitch among TSV arrays is designed in the structure. The diameters for the TSVs and the microjoint bonding area are 30 and 50 μm, respectively. After assembling each 10-μm-thick ultra-thin chip, the gap filled by the underfill to enhance the structural strength of the microjoints is approximately 15 μm. Molding material is present in the peripheral region of the stacked chips.

3. Stress simulation modellings

In addition to the performance of 3D nonlinear FEA, a quarter symmetry of the entire structure is constructed given that the layout arrangement of 3D-IC packages is in-plane biaxial symmetry. Hence, the

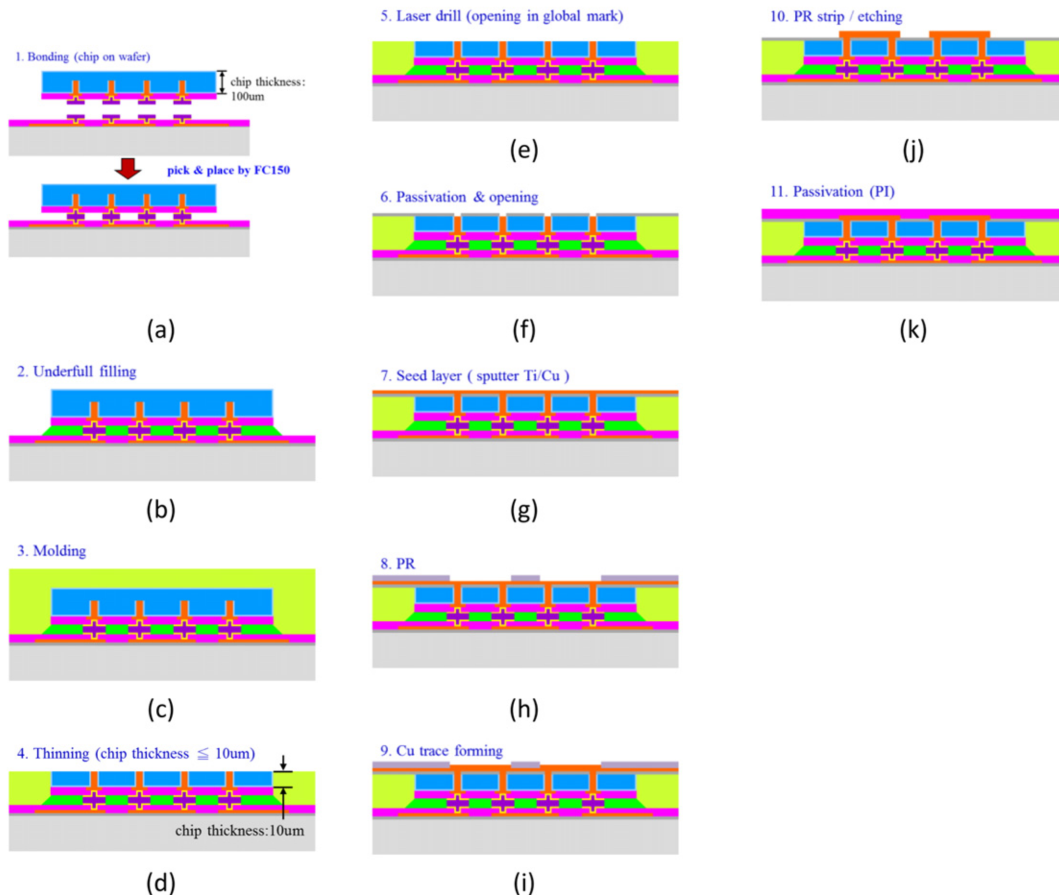

Fig. 2. Explanations for chip stacking process flows in the 3D-IC packaging structure.

Download English Version:

https://daneshyari.com/en/article/544141

Download Persian Version:

https://daneshyari.com/article/544141

Daneshyari.com