



Dielectric liner reliability in via-middle through silicon vias with 3 Micron diameter



Yunlong Li ^{a,*}, Stefaan Van Huynenbroeck ^a, Philippe Roussel ^a, Mohand Brouri ^b, Sanjay Gopinath ^c, Daniela M. Anjos ^c, Matthew Thorum ^c, Jengyi Yu ^c, Gerald P. Beyer ^a, Eric Beyne ^a, Kristof Croes ^a

^a Imec, Kapeldreef 75, B-3001 Leuven, Belgium

^b Lam Research Corporation, Kapeldreef 75, B-3001 Leuven, Belgium

^c Lam Research Corporation, 4650 Cushing Parkway, Fremont, CA 94538, USA

ARTICLE INFO

Article history:

Received 8 July 2015

Received in revised form 20 January 2016

Accepted 25 January 2016

Available online 28 January 2016

Keywords:

High aspect ratio through silicon via
Sidewall roughness
Atom Layer Deposition
Dielectric reliability
Local field enhancement
Bimodal distribution

ABSTRACT

In high aspect ratio through silicon vias (TSV's), the trench step coverage (conformality) of liner, barrier and seed is critical for both the process integration and reliability. If the conformality of a deposition process is improved, the required thickness to be deposited on the field of the wafer can be reduced. Consequently, less material needs to be removed by CMP on the field, which reduces the manufacturing cost. In this paper, the reliability of two liner/barrier/seed options, which were successfully integrated into via-middle TSV's with a diameter of 3 μm and an aspect ratio (AR) of 17 is investigated. Both controlled ramp rates (IV_{ctrl}) as well as standard Time Dependent Dielectric Breakdown (TDDB) at 100 °C were employed as electrical testing methods to investigate the dielectric and barrier reliability properties of the studied systems. The first studied system consists of a non-conformal CVD O₃ TEOS oxide liner, an ALD TiN barrier and a PVD Cu seed. The second studied system employs a conformal ALD oxide liner, a thermal ALD WN barrier and an ELD NiB seed. Both studied systems show excellent reliability properties. Scalable highly conformal liners are more sensitive to local field enhancement at the high fields applied during highly accelerated tests which are far above normal operation conditions. Their performance at lower fields, however, still meets standard reliability specifications.

© 2016 Elsevier B.V. All rights reserved.

1. Introduction

Via-middle through silicon via (TSV), is a promising method to enable stacked integrated circuits (3D-SIC) [1]. The via-middle TSV's are integrated prior to the BEOL structures. A typical filling sequence for a copper TSV is a) liner deposition, where the liner acts as a dielectric isolation between the Si and the Cu, b) barrier deposition to prevent copper drift into the liner, c) seed deposition and subsequent plating and d) CMP to remove the overburden after plating.

TSV's with a diameter of 5–6 μm are becoming mature. There is a continuous strive for smaller TSV's. The main reason is that smaller diameter TSV's occupy less space and have smaller keep-out-zones [2]. The TSV-depth is usually not scaled because the mechanical stability of the wafer and eventually of the dies deteriorates rapidly if the thickness is further reduced. For this study, TSV's with a diameter of 3 μm and a depth of 50 μm (3 \times 50 μm , AR = 17) were developed.

This paper addresses the electrical reliability of TSV's filled with two different TSV filling options compatible with 3 μm diameter TSV's, further referred to SYS1 and SYS2, where SYS1 uses the more traditional medium to low step coverage liner and seed technologies and SYS2

employs highly conformal liner, barrier, and seed deposition technologies. The electrical reliability of the liner itself as well as the reliability of the barrier were assessed independently. The reliability criterion for the liner is the breakdown strength towards the applied field during operation. The barrier needs to prevent copper drift into the liner at operating fields and temperatures.

2. Experimental

Table 1 shows the details of the samples used in this study. Two samples with 5 \times 50 μm TSV's were used as reference [3]. The REF1 samples had a PVD Ta barrier and a PVD Cu seed deposited on a non-conformal O₃ TEOS liner. This system has an electrically reliable liner and a bad barrier [4]. Instead of the PVD Ta barrier, the REF2 samples had a PVD Ti barrier, where this systems had good liner and barrier properties [3]. The first experimental system (SYS1) has a non-conformal CVD O₃ TEOS liner, an ALD TiN barrier and PVD Cu seed. The second experimental system (SYS2) has a conformal ALD liner, a thermal ALD WN barrier and an ELD NiB seed.

Electrical charges present in the liner were quantified using CV-measurements: When sweeping from a positive to a negative voltage, the MIS-system (with p-Si substrate) goes from depletion to accumulation. The voltage at which this transition happens, the so-called flatband

* Corresponding author.

E-mail address: yunlong.li@imec.be (Y. Li).

Table 1
Studied TSV-filling options (units: micron).

Split	Dim	Liner	Barrier	Seed
REF1	5 × 50	O ₃ TEOS	PVD Ta	PVD Cu
REF2	5 × 50	O ₃ TEOS	PVD Ti	PVD Cu
SYS1	3 × 50	O ₃ TEOS	ALD TiN	PVD Cu
SYS2	3 × 50	ALD SiO ₂	Th. ALD WN	ELD NiB

voltage shift V_{FB} , is indicative of the amount of charges present in the liner: the higher the V_{FB} , the more the charges are present.

The electrical reliability of the liner and the capability of the barrier to prevent copper diffusion were studied using IV_{ctrl} and TDDB at 100 °C [5]. Both methods allow the estimation of the field acceleration factor γ of the E-model, a model which is often used to link dielectric breakdown times (t_{BD}) with field E : $t_{BD} \propto \exp(-\gamma E)$. The IV_{ctrl} -method, which is a faster method than TDDB, estimates γ through measuring the breakdown field EBD for different ramp rates R : $E_{BD}(R) \propto \ln(R)/\gamma$. TDDB allows to estimate γ by directly measuring t_{BD} at different fields. By looking into the distribution of failure times at a given field, TDDB also allows to detect different failure modes and to estimate the lognormal shape parameter σ for each mode.

The liner reliability was studied by applying a negative voltage to the TSV (later referred to as copper confined mode). In this stress mode, the TSV copper ions are attracted by the voltage source and are not injected into the liner during the test. This allows the study of intrinsic liner properties. Barrier properties were studied by comparing measurements in the copper confined mode by those obtained when applying a positive voltage to the TSV (later referred to as copper driven mode). In the latter stress mode, copper ions are pushed into the liner in case of a defective barrier. Big differences in IV_{ctrl} and TDDB data between both modes could indicate bad barrier properties. Fig. 1 illustrates the differences between copper confined and copper driven modes.

3. Results and discussion

The results of the IV_{ctrl} and TDDB measurements are summarized in Table 2. The REF1 and REF2 splits were discussed in detail in Refs. [3–4]. The low V_{FB} of REF1 is explained by H-outgassing through the PVD Ta,

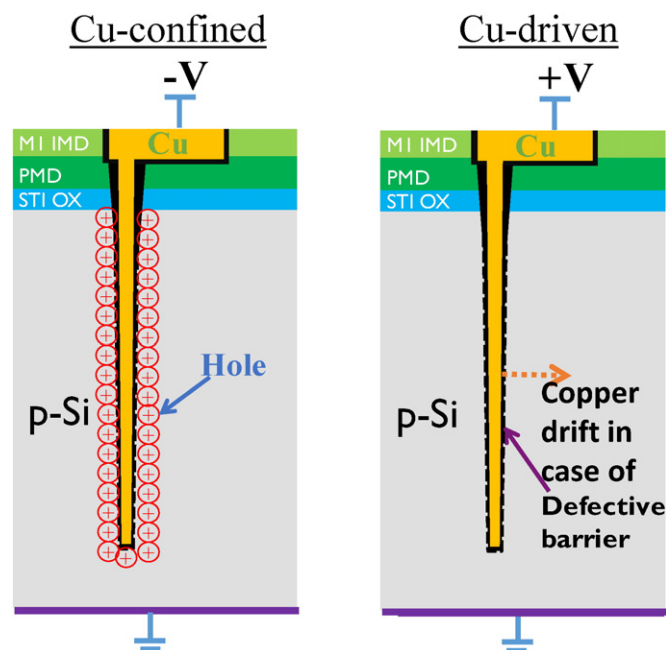


Fig. 1. Configuration difference between copper confined and copper driven modes.

Table 2
Reliability results of studied TSV-filling options.

Split	V_{FB} (V)	γ for IV_{ctrl}		TDDB	
		-V	+V	-V	+V
REF1	2	High	Low	High γ , high σ	Mode 1: high γ , high σ Mode 2: low γ , low σ
REF2	10	High	High	High γ , high σ	High γ , high σ
SYS1	20	High	High	High γ	Medium γ , high σ
SYS2	1.5	High	High	Mode 1: high γ , high σ Mode 2: high γ , low σ	Medium γ , medium σ

leading to the weak barrier properties [4] as detected by the low γ from the IV_{ctrl} -measurements in the copper driven mode. The first mode of the TDDB failure times had a high γ and a high σ , which indicated intrinsic liner breakdown. The low γ and a low σ of mode 2 indicated copper injection. The high γ in the copper confined mode suggested good intrinsic liner properties for both systems. The high γ and high σ in the copper driven mode for the REF2 samples also suggested good barrier properties. The high V_{FB} for these samples was explained by the fact that the H was kept in the liner itself [4]. Note that the high σ 's of the tests leading to intrinsic liner breakdown were explained by a high non-uniformity in liner thickness induced by the scallops in the TSV sidewall.

As the reliability data of our first experimental system, SYS1, shows the exact same trends as the REF2 system, we believe that the same mechanisms play a role: the H is kept within the liner and does not diffuse into the barrier, where the liner and barrier properties are good.

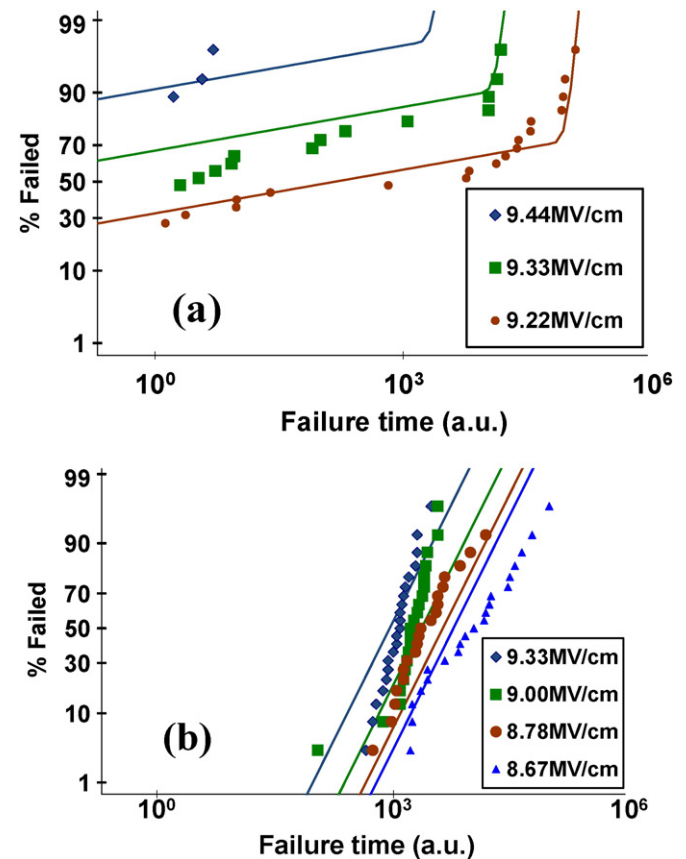


Fig. 2. Lognormal probability plot and maximum likelihood statistical E-model fitting of the TDDB failure times obtained on SYS2 (a) in the copper confined mode and (b) in the copper driven mode.

Download English Version:

<https://daneshyari.com/en/article/544143>

Download Persian Version:

<https://daneshyari.com/article/544143>

[Daneshyari.com](https://daneshyari.com)