



The impacts of fabrication error in Si wire-waveguides on spectral variation of coupled resonator optical waveguides



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ABSTRACT

We experimentally investigate the impacts of fabrication error in Si wire-waveguides on the spectral variation of 5th-order coupled resonator optical waveguides (CROWs). In the fabrication of these waveguide devices, 40-nm-node CMOS technology with ArF immersion lithography was used. The characterization of the CROWs was done by using an automatic optical wafer-level probing system. As for the fabrication errors in 440-nm-wide/220-nm-thick waveguides, standard deviations in waveguide cross-sectional size for a single 300-mm wafer were confirmed to be 0.83 nm in width and 0.24 nm in height. The fabricated CROWs in a single wafer exhibited quite similar resonant peak shapes to each other, and also showed a remarkably small standard deviation of 0.67 nm in resonant wavelength, which agrees with the theoretical estimation from the fabrication error. These results show that the precise process control using ArF immersion lithography technology is effective to the reproducible device fabrication for wide-bandwidth optical interconnection.

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1. Introduction

Optical integrated circuits using silicon photonics technology have been expected as a solution to overcome bandwidth bottleneck both in data transmission among LSIs and in long haul communication [1–3]. Applying existing CMOS process technology to the fabrication of such optical ICs will give a shortcut to a low cost production. Most of fabrication processes for the silicon photonic devices are compatible to CMOS [4–6], and process technology and methodology related to semiconductor devices are, therefore, useful for the photonic circuit. Nevertheless, it is noteworthy that, in silicon photonics, fabrication errors, such as line edge roughness (LER) and deviations from designed width (σ_w) and height (σ_H) in optical silicon waveguides should be more accurately controlled, because the LER in waveguide causes scattering loss of propagating light [7–10] and deviations in waveguide dimension result in the degradation in transmission spectrum of optical devices. Especially, in multi/demultiplexers for wavelength-division multiplexing (WDM) system, random optical phase error caused by the fabrication error in waveguide width and thickness degrades device performance [11–14].

In the previous papers [13–16], we have already reported the phase errors were greatly reduced by using 40-nm node technology with high-resolution ArF immersion lithography, and as the results, the

quality of the transmission spectra in multi/demultiplexers, such as arrayed waveguide gratings (AWGs) [15–16], CROWs [13], and Mach-Zehnder interferometers (MZIs) [14] were dramatically improved, in the comparison with the device fabricated by using 130-nm node and 90-nm node CMOS technologies. As for the 5th-order CROWs fabricated by using ArF immersion lithography [13], the observed flat-top resonant peak shape was almost the same as the designed one, although the fabrication by 130-nm node technology with dry KrF lithography resulted in the serious deformation of the peak shape due to the phase error. The phase error, $\sigma(\delta\phi)$ in case of ArF immersion lithography was estimated to be about 0.03π , which was less than 1/6 of that in dry KrF immersion lithography. It was also reported that the range of spectral shift for 6 CROW devices on a single 300-mm wafer was about 3.6 nm [13]. The aims of this paper are twofold; one is to examine whether the device performance in multi/demultiplexers fabricated by 40-nm node technology can be assured for all devices in a single 300 mm ϕ wafer, and the second is to experimentally clarify the relationship between the fabrication error and the reproducibility. In this study, as a representative of multi/demultiplexers, the CROWs were used for the investigation.

In the following sections, we first describe the fabrication of optical devices using 300 mm ϕ SOI wafers and device characterization by an optical wafer-level probing system, and then present the results of fabrication error of Si wire-waveguides and the wafer-level reproducibility of the CROW performance. On the basis of the results, we discuss how the reproducibility of the optical device performance is affected by the fabrication error.

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2. Experimental

The 5th-order CROWs were fabricated on a 300-mm ϕ silicon-on-insulator (SOI) wafer having a 220-nm-thick silicon top layer and a 2- μ m-thick buried oxide (BOX) layer [10]. The number of the CROW is 58. The waveguide core pattern with a width of 440 nm for the CROW was formed by applying ArF immersion lithography and anisotropic inductively coupled plasma etching to the silicon top layer, and then a 2- μ m-thick SiO₂ film was deposited on the waveguide pattern as a cladding layer.

The design for a test element of the 5th-order CROW with grating couplers (GCs) as optical I/O is shown in Fig. 1. As for the CROWs, the curvature radius and the directional coupling length for each ring were 6 μ m, and 5 μ m, respectively. The gap between rings was a constant value of 200 nm. The GCs consisted of a constant pitch grating of a 620 nm in grating pitch, and a 70 nm in half-etched depth.

An automatic wafer-level probing system including optical I/O was applied to the characterization of CROWs. In the system, a couple of polarization-maintaining optical fibers on probing head were optically connected to the CROW device under test on the wafer through a couple of GCs during measurement, as shown in Fig. 2. In the alignment sequence for measurement, a couple of probing fiber ends are automatically aligned on corresponding GCs as maximizing the returning power of a probing light.

Before the characterization of the CROWs, it was confirmed that the coupling loss between the GC and the single mode fiber showed a minimum at λ of 1.55 μ m, and -3 dB excess loss bandwidth was about 60 nm. The measurement accuracy of the optical coupling between the GC and the fiber was estimated to be a small value about 0.1 dB, in reputation by the automatic measurement, and, on the other hands, the wafer-scale variability in the coupling loss for a single 300-mm wafer in this work was 0.15 dB. It was reported that the coupling efficiency varies by the fabrication error in dry etching depth for the grating formation [17], and so, the observed small difference between the measurement accuracy and wafer-scale variability for the coupling loss implies that the wafer-scale uniformity of grating depth was kept to be a low level.

3. Results and discussions

3.1. Fabrication errors in Si wire-waveguides

Fig. 3 shows the SOI thickness deviation of a 300 mm ϕ SOI wafer which was used for the fabrication of the CROWs. The standard deviation of SOI thickness was 0.24 nm. Because etching amount from the top of the SOI layer in the fabrication of the waveguides is less than a

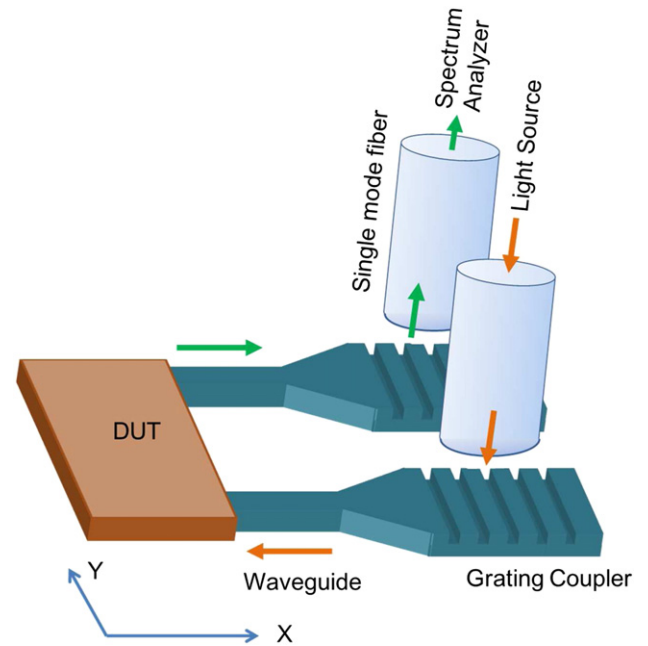


Fig. 2. Schematic configuration of an optical wafer-level probing system.

several nm, the initial variation of SOI thickness should be kept. As for width deviation for the fabricated waveguides, the standard deviation σ_w is 0.83 nm for a single wafer. We also evaluated chip-scale width deviation, because random phase error which degrades transmission spectrum of multi/demultiplexers should be related to the width variation within short distance (typically 1 ~ 10 mm). As shown in Fig. 4, the standard deviation of chip-scale width variation σ_{w_chip} is shown to be 0.47 nm for the length of 10 mm. As for LER, in our recent papers about the low propagation loss of silicon wire waveguides fabricated

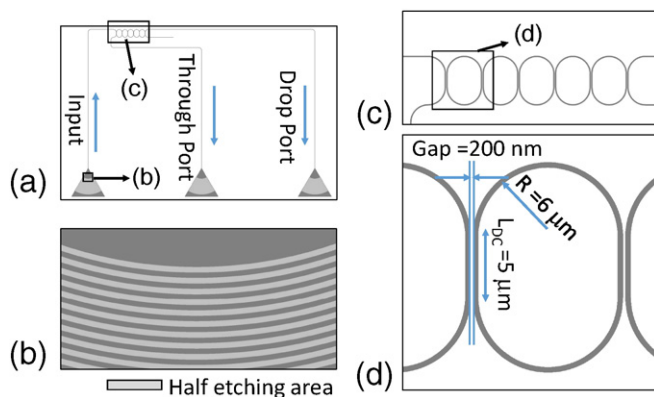


Fig. 1. (a) The schematic design for a test element of a 5th-order CROW with grating couplers (GCs) as optical I/O, (b) the design image of grating area for optical coupling, (c) the configuration of the 5th-order CROW, and (d) detailed design showing the configuration of the rings.

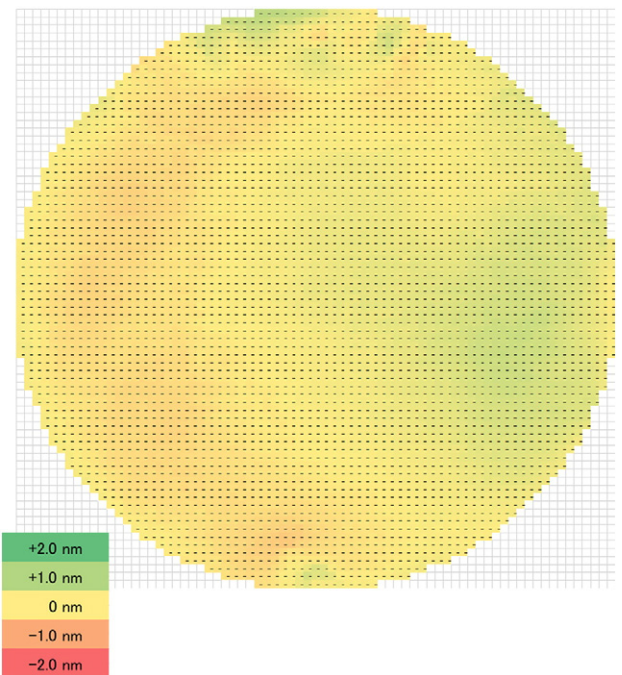


Fig. 3. The SOI thickness deviation of 300 mm ϕ SOI wafer which was used for the fabrication of the CROWs. The average value, the standard deviation, and the deviation range (the maximum–the minimum) for SOI thickness were 224.5 nm, 0.24 nm, and 1.37 nm, respectively, as the results of the measurement for more than 4000 points in a single wafer with wafer edge exclusion of 6 mm.

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