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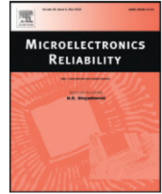

Accurate lifetime prediction for channel hot carrier stress on sub-1 nm equivalent oxide thickness HK/MG nMOSFET with thin titanium nitride capping layer

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ABSTRACT

Channel hot carrier (CHC) degradation in sub-1 nm equivalent oxide thickness (EOT) HK/MG nMOSFET has been studied in this paper. It is found that the degradation can be divided into two regimes based on stress induced drain-induced-barrier-lowering (DIBL) variation, namely higher stress drain voltage regime and lower stress drain voltage regime. Cause of the division is attributed to different activities of hot carriers. Lifetime prediction excluding higher voltage regime shows to be a more accurate method. In addition, there exists a deviation of degradation trend between 1.4 nm TiN and 2.4 nm TiN thickness nMOSFET in lower voltage regime. The deviation is attributed to different interface trap generation induced by TiN capping layer in different thickness, which is proved by the charge pumping experiment.

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1. Introduction

Reliability issues always play an important role in development of MOSFET technology [1–2] and are becoming more and more difficult and important due to the complicated high-k/metal gate (HK/MG) band structure. HK/MG is one of key technologies in current and future MOSFET technology node. Hence, a good and sufficient knowledge of reliability problems in HK/MG is necessary. Channel Hot Carrier (CHC) degradation, one of the major reliability issues, has a critical impact on MOSFETs even in a supply voltage below the threshold energy of hot carriers [3–6]. CHC degradation brings about shift of a series of parameters, among which DIBL variation can reflect local trapping of carriers [7].

Among various potential candidates for metal gates, refractory metal nitrides have been intensively studied and TiN metal gate has received tremendous interests [8–9]. However, there are few systematic studies about TiN capping layer impact on CHC reliability. In this work, CHC reliability of nMOSFETs with different atomic layer deposition (ALD) TiN thickness is studied. It is found that in both long and short channel devices the degradation can be divided into two regimes based on our DIBL model [7]. The division is attributed to different activities of hot electrons. In lower voltage regime there is a deviation of degradation trend between two different ALD TiN thicknesses, which is attributed to abnormal interface generation. Charge pumping experiment data verified the abnormal interface generation due to different TiN thickness.

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2. Material and methods

HK/MG nMOSFET fabricated by full gate-last process was used in the test devices. For gate-last process devices, the O-zone method was used to grow ultra-thin oxides as IL after standard cleaning procedures. Then, HfO_2 films were deposited by ALD with sequentially post deposition annealing. Next, 1.4 nm ALD TiN and 2.4 nm ALD TiN were grown for two kinds of nMOSFETs respectively, followed by a series of multi-layers metal gate stack procedures for HK/MG gate optimization. CHC degradation was evaluated by a conventional measurement-stress-measurement approach. Test was executed in room temperature with various stress modes. Total stress time is 1000 s. Time-to-fail (TTF) for devices is determined by 10% degradation of drain current in saturation region (I_{dsat}). Through C–V measurement the flat band voltage and equivalent oxide thickness (EOT) were extracted. C–V results show that an EOT of nearly 8.5 Å and a flat band voltage of nearly −0.8 V were achieved in both 1.4 nm and 2.4 nm TiN nMOSFETs. Gate length (L_G) of long and short channel MOSFETs is 350 nm and 50 nm. Gate width of long and short channel MOSFETs is 8 μm and 3 μm respectively. Long channel devices with different TiN thickness have about the same threshold voltage (Vth) between 0.35 V and 0.37 V. The Vth values of short channel devices also have little difference, which is 0.025 V at most due to additional effects. The electrical characterizations of nMOSFETs in equal gate length are almost the same. DIBL is defined as follows: [10].

$$DIBL = -(V_{th,sat} - V_{th,lin})/(V_{Dsat} - V_{Dlin}) \quad (1)$$

$V_{Dsat,}$ V_{Dlin} are drain voltage (V_D) when transistor works in saturation region and linear region respectively, which are set at 1.0 V, 0.05 V. $V_{th,sat}$, $V_{th,lin}$ are the threshold voltage in saturation region and linear region respectively. I_{dsat} is measured at $V_G = V_D = VDD = 1$ V.

3. Results and discussion

In Fig. 1, relations between substrate current (I_{sub}) and gate voltage (V_G) for both long and short channel nMOSFETs with different TiN thickness are compared. It shows that there exists a peak for each $I_{sub} \sim V_G$ curve, even in 50 nm short channel device. The peak relates to the maximum impact ionization. Hence, degradation under peak I_{sub} CHC stress condition is explored in this work.

Fig. 2 depicts TTF ~ V_G for both long and short channel devices with 1.4 nm and 2.4 nm TiN respectively. Stress drain voltage (V_D) was set at a series of 1.7 V to 2.5 V. Then stress V_G was set at voltage corresponding to peak I_{sub} and TTF was extracted. It shows that TTF-I_{sub} curves follow the power law, which is consistent with Eyring Model in the JEDEC standard [11]. Our devices are designed to work at VDD of 1 V. But the TTF under 1.7 V stress drain voltage is extrapolated to compare the experiment result more easily and obviously. First, TTF of devices under stress $V_D = 1.7$ V is extrapolated based on the universal TTF-I_{sub} curve from stress $V_D = 1.8$ V to 2.5 V, shown as open pentangles and open diamonds. Second, actual experimental TTF under $V_D = 1.7$ V is added to Fig. 2(a)(b) shown as the left most solid pentangles and solid diamonds. It shows that there exists a big gap (shown as red arrows) between extrapolated and experimental value in 1.4 nm TiN devices and a relatively narrow gap in 2.4 nm TiN devices. Therefore, lifetime prediction from universal TTF-I_{sub} curve is not very accurate.

At the same time, DIBL variations of both long and short channel nMOSFETs under a series of different drain voltage stress conditions are compared in Fig. 3. $DIBL_0$ refers to the DIBL of fresh devices. It shows that DIBL has a slight increase under relatively lower drain voltage stress (1.8 V to 2.1 V, Lower V_D stress), while DIBL has a significant increase under relatively higher drain voltage stress (2.2 V to 2.5 V, Higher V_D stress). According to our previous report [7] significant increase of DIBL implies that there exists significant trapping of carriers in the oxide near the drain side, namely the hot electrons. Thus, under Higher V_D stress the impact of trapped charge in the oxide (N_{ot}) becomes more important, while under Lower V_D stress the main cause of degradation is the interface traps (N_{it}). To further confirm the situation the charge pumping measurements are performed at different frequencies as shown in Fig. 4. The pulse amplitude is 1.2 V. To obtain accurate charge pumping current, the primarily measured charge pumping current are subtracted by charge pumping current at a low frequency 10 Hz according to previous report [12]. Based on the report before [13], Fig. 4 connotes that slow state traps increase significantly after 1000 s Higher V_D stress while there are almost no slow state traps increasing after Lower V_D stress. The distinction connotes that the two kinds of situations need to be considered separately.

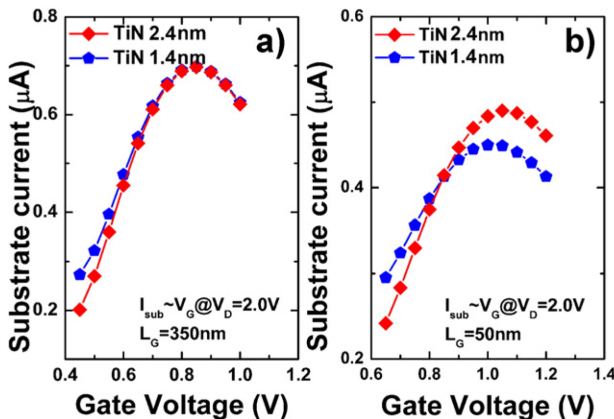

Fig. 1. Relation between substrate current and gate voltage with drain voltage 2.0 V. Peak substrate current exists both in long and short channel devices.

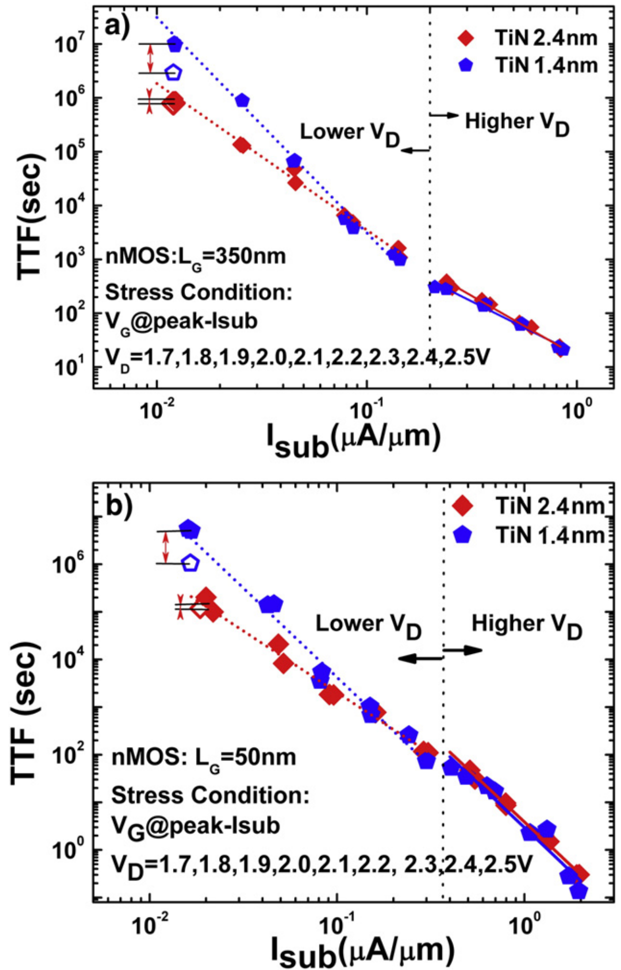

Fig. 2. Relation between TTF and substrate current for a)long and b)short channel length devices with different TiN thickness. The open pentangles and diamonds represent extrapolated TTF at 1.7 V based on universal TTF-I_{sub} (1.8 V to 2.5 V). The leftmost solid pentangles and diamonds in a)b) refer to actual TTF of 1.7 V. The dash lines refer to predicted TTF based on Lower V_D stress (1.8 V to 2.1 V) TTF-I_{sub} only.

Then TTF-Isub curves are divided into two regimes as depicted in Fig. 2, namely Higher V_D and Lower V_D. Under Higher V_D, 1.4 nm and 2.4 nm TiN nMOSFETs almost have the same degree of degradation. However, under Lower V_D, TTF curve of 1.4 nm TiN devices has a steeper slope than 2.4 nm TiN devices. Reliability of 1.4 nm TiN devices gradually shows better than 2.4 nm TiN at lower substrate current. The reason for the difference is explained as follows. As shown in Fig. 5(a), energy of hot electrons under Lower V_D is relatively lower than Higher V_D. Under Lower V_D, hot electrons mainly interact with the interface between IL and substrate, resulting in generating of interface trap [14]. But under Higher V_D, hot electrons can inject or/and tunneling to dielectric layer, as shown in Fig. 5(b). Trapping of hot electrons becomes dominant under Higher V_D, covering the distinction of TTF between 1.4 nm and 2.4 nm TiN devices only induced by interface trap. This is consistent with the DIBL model [7] and DIBL results in Fig. 3. In Fig. 6, to compare the reliability more accurately, I_{dsat} degradation after 1000 s Higher V_D CHC stress is directly plotted versus the corresponding peak I_{sub}. It shows again that there is not much difference between 1.4 nm and 2.4 nm devices in both long and short channel devices.

After the division of Higher V_D and Lower V_D, TTF is extrapolated from the curve under Lower V_D (1.8 V to 2.1 V) only, namely the dash lines shown in Fig. 2. Compared to extrapolated points base on universal

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