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A concise study of neutron irradiation effects on power MOSFETs and IGBTs☆

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ABSTRACT

Over the past years there have been growing concerns on the adverse effects of atmospheric neutrons on power semiconductors even at sea level. In this paper we report recent results of neutron irradiation (1.9 MeV) experiments conducted on 650 V Super-Junction MOSFETs and Field-Stop Trench Insulated Gate Bipolar Transistors (IGBTs). The typical experiments found in literature which study the irradiation of power electronics chose a white line spectrum of neutron energies, ranging from 1 to 180 MeV; however, we have deliberately chosen to study the effect of monochromatic radiation of fast neutrons, as a first in a series of experiments, to better understand the full range of interactions from fast to ultra fast neutrons (100 MeV). We show that a multitude of failure modes already appear at neutron energies of 1.9 MeV ranging from gate oxide degradation to single event effects (SEE). Moreover an outstanding ruggedness of devices is demonstrated, which shows no failures at 80% rated break down and below under extreme aging conditions.

1. Introduction

The move to electro-mobility, alternative energies and a general attitude towards energy consciousness has brought upon a renaissance of power electronics [1–4]. Switching high voltages and currents makes power electronics very different than conventional MOSFETs, with more complex structures and physics. Given the relatively young age of power electronic devices, much of their switching and robustness characteristics still remain to be understood. Given the broad range of new safety critical applications for power electronics, such as electrical vehicles, power grids, server farms and avionics it has become important to analyze and study the effects of environmental hazards on the longevity of these devices. Among these hazards are damages resulting from the cosmic radiation [5–11], at and above sea-level. Due to spallation processes in the atmosphere the largest portion of impinging particles, at altitudes relevant to non-avionic applications, are so called atmospheric neutrons [12]. Atmospheric neutrons are usually, depending on which literature one consults [7,6,12,13,15], in the range of 1–200 MeV. Besides cosmic radiation, lightning can also generate atmospheric neutrons with similar energy ranges. When such atomic particles hit a power device with sufficient energy it can lead to an elastic collision, as seen visualized in Fig. 1. The incoming neutron can collide in one of two ways, elastic and inelastic. Fast neutrons, those in the MeV and above energy range, account for most of the elastic collision. In such collisions ions can be knocked out of the crystal lattice, that is at the foundation of each semiconductor device, the atom being knocked-off in turn creates electron–hole pairs along its trajectory through the lattice [14]. These displacements, and charge-plasmas can cause a multitude of failure modes, namely Single Event Burnout, total ionizing dose damage and Single Event Gate Rupture [5–7,13,16,17]. Most experiments focus on determining the failure rate of devices bombarded by a white line energy spectrum of neutrons, mimicking the JDEC [15] published energy distribution of neutrons at sea level. In this experiment we have consciously chosen to use mono-chromatic neutrons at 1.9 MeV which resembles one of the most probable neutron energies at sea level. Further as this is a primary to further investigations, to better understand the radiation-technology interaction it is essential to understand the effect of energy on damage.

2. Experimental

For the irradiation experiments two technologies where chosen, Fairchilds SuperFetII 650 V and 650 V Field Stop 3 Trench IGBTs. From each technology 96 devices were selected (96 IGBTs and 96 MOSFETs), these where then split into a control and an irradiation group each consisting of 48 devices. Prior to irradiation each devices was subject to multiple electric tests, namely determining the breakdown voltage $BV_{DSS/CES}$ at the data sheet specified current, the gate leakage I_G and the threshold voltage V_{th}. A total of two tests boards where made to mount the devices for the experiment, see Fig. 2. The boards consist of four rows, each row is biased at a different voltage, 0 V, 390 V, 520 V and 650 V (0, 60, 80 and 100% BV respectively). In each of the rows

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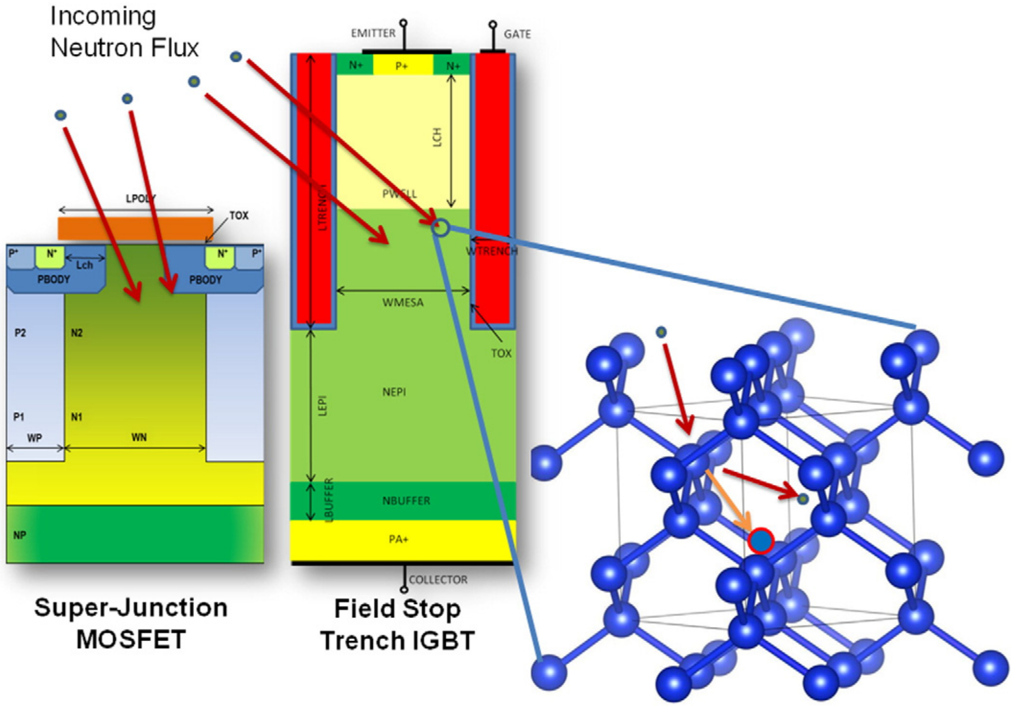

Fig. 1. Schematic representation of impinging neutrons on a Super-Junction power MOSFET (left) and an IGBT (right).

twelve devices in a D^2-Pack are mounted on the front side and the monitoring circuit on the back side (Therefore neutrons are at an incidence angle to the front side of the package). In order to detect a failed device, LEDs (VLMS30K1L2-GS08) are mounted on the backside of the board, with current limiting resistors in series. These indicate when a device falls out and has a leakage current of at least 2 mA (which is in excess of both IGBT (1 mA) and MOSFET (0.25 mA) specifications at breakdown. See Fig. 2. The resistors limit the current to a maximum of 2 mA, which is the nominal current for the LEDs to glow. This also prevents failed devices from being fully destroyed. Two LEDs were

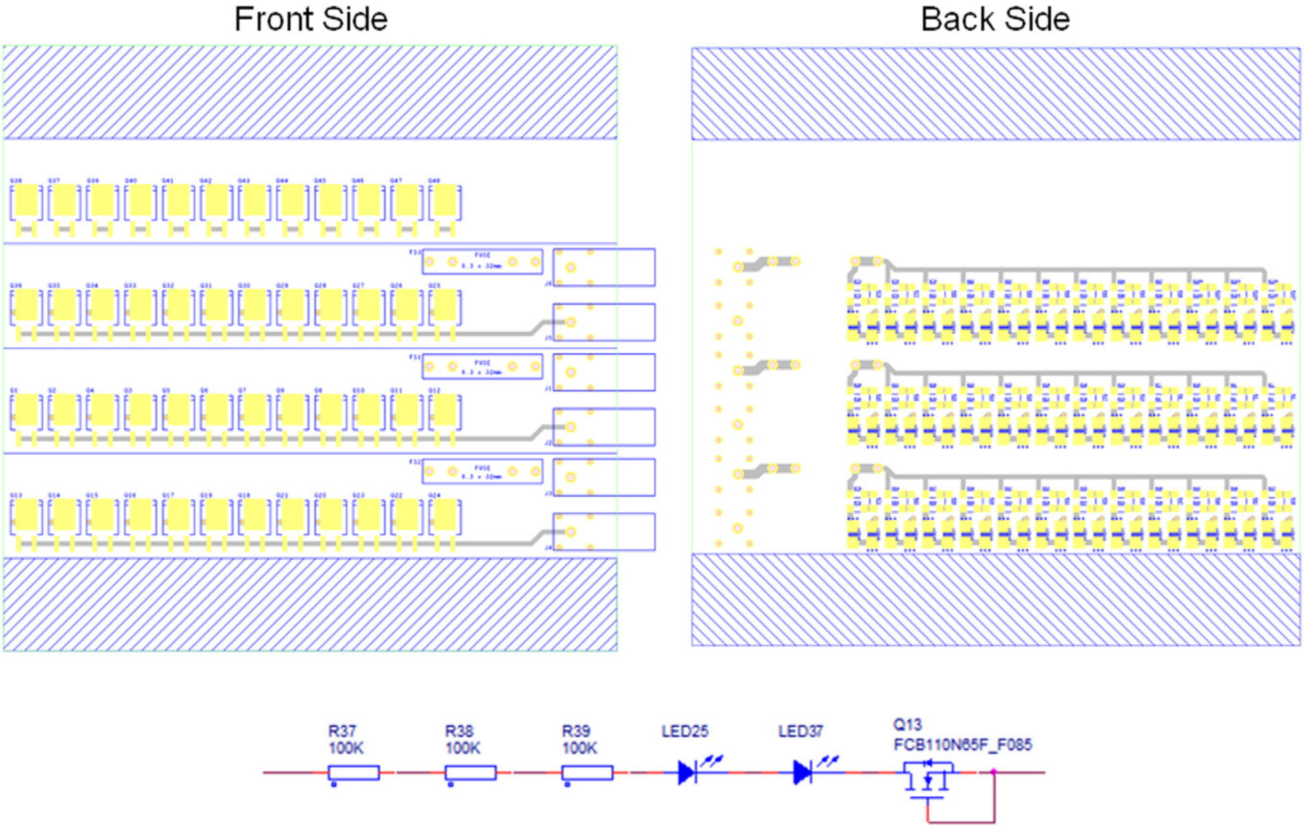

Fig. 2. Layout and circuit schematic of the test boards used for both MOSFETs and IGBTs. The rows are biased (from top to bottom) at 0, 390, 520 and 650 V respectively. As a fail-safe two LEDs are mounted per device and series resistors further limit the leakage current.